Product Specification | Rev. 3.0 | 2015

IMME256M64D3SOD8AG (Die Revision E)
2GByte (256M x 64 Bit)

2GB DDR3 Unbuffered SO-DIMM
By ECC DRAM
RoHS Compliant Product

Version: Rev. 3.0, JUL 2015

3.0 – Remove option of Speed Grade at PC3-12800

Version: Rev. 2.0, MAY 2015

2.0 – Remove option of Operating Voltage at 1.35V

Version: Rev. 1.0, FEB 2015

1.0 - Initial release

Remark:
Please refer to the last page of the i) Contents ii) List of Table iii) List of Figures .

We Listen to Your Comments

Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to: sales@intelligentmemory.com

Features

- 204-Pin Unbuffered Small Outline Dual-In-Line Memory Module
- Capacity: 2GB
- JEDEC-Standard
- Built by ECC DRAM Chips
- Bi-directional Differential Data-Strobe
- 64 Bit Data Bus Width without ECC
- Programmable CAS Latency (CL):
    - PC3-10600: 5, 6, 7, 8, 9, 10
- Programmable CAS Write Latency (CWL):
    - PC3-10600: 5, 6, 7
- Programmable Additive Latency (Posted /CAS): 0, CL-2 or CL-1(Clock)
- On-Die Termination (ODT)
- ZQ Calibration Supported
- Burst Type (Sequential & Interleave)
- Burst Length: 4, 8
- Refresh Mode: Auto and Self
- 8192 Refresh Cycles / 64ms
- Asynchronous Reset
- Gold Edge Contacts
- 100% RoHS-Compliant
- Standard Module Height: 30.00mm (1.181 inch)

ECC DRAM Introduction

Special Features (ECC – Functionality)

- Embedded error correction code (ECC) functionality corrects single bit errors within each 64 bit memory-word.
- The error correction is performed automatically inside the ECC DRAM device.
- Parity data is generated by an internal ECC logic and then stored in additional, dedicated memory space
- Fully compatible to JEDEC standard DRAM operation and timings
- JEDEC compliant FBGA package (drop in replacement)

ECC – Functionality / Challenges and Achievements

During the production test, the ECC DRAMs are verified to pass extensive burn-in, core-function and speed tests throughout the complete memory array, including the memory-space for the parity-data. Only when every single memory cell has passed these tests, the ECC function is switched on by hardware and the products get shipped. With the ECC function activated, customers will have unparalleled functionality and quality.

Embedded ECC functionality

Intelligent Memory ECC DRAMs are JEDEC compliant components with integrated error-correction. The internal logic automatically detects and corrects single-bit-errors "on the fly" without any delays or additional latencies compared to conventional DRAM components. ECC DRAMs have additional memory-space to store the ECC-check-bits. Internally, the ECC DRAM works with a 72 bit wide buffer. When writing to the DRAM, an additional 8 ECC check-bits are being generated per each 64 bit data-word. Upon a Read-command, the whole 64+8 bit word is transferred to the buffer and automatically corrected by an ECC Hamming Code (72, 64). The corrected data is then applied to the DQ lines of the ECC DRAM in bit-widths of 4, 8, 16 or 32 bit, depending on the organization of the device.

The ECC algorithm is able to detect and correct one bit-error per 64+8 bit data-word. A 1 Gigabit ECC DRAM component has 16,777,216 data-words of 64 Bits. In each of these data-words, one single-bit error could be corrected, resulting in approximately 16 million times higher reliability of ECC DRAM compared to a conventional DRAM with similar capacity.

Note: If Burst Length x DRAM-I/O-width < 64 bit during a Write-command, the ECC-functionality is limited. Please contact Intelligent Memory for further details.

Comparison to conventional ECC implementation

ECC error correction is very common on high end industrial applications and servers. It normally requires an ECC-capable memory-controller which has an extra-wide data-bus with for example 72 bits (64 data-bits + 8 check-bits). The memory controller generates the required additional check-bits for the data and writes the extra wide data-word to the memory. Upon a Read-command, the memory controller will verify the data-integrity of the data-word + check-bits and performs the correction algorithm. Performing this algorithm affects the systems performance. In addition to the requirement for an ECC-capable memory controller, the conventional way of ECC correction requires multiple DRAMs to be accessed in parallel to achieve the extra-wide bit-width. On Server-memory-modules, for example, 18 DRAM-components with 4 data-lines each are put in parallel to reach the total 72 bit extra-wide data-bus.

With IM ECC DRAM, the check-bit-generation, verification and correction is performed inside the memory device. Every single ECC DRAM performs the error correction by itself, thus it does not require ECC-capable processors/controllers nor any wide data-bus between the controller and the DRAM. Because the ECC DRAM components are JEDEC compliant, they are drop-in replacements to conventional DRAM-memory. Any existing application that is currently built with conventional DRAM can be equipped with error-correction functionality. Note that, if a standard 64 bit memory-module is built using ECC DRAMs, the depth of error-correction is deeper than on 72 bit ECC memory module as each DRAM component on the module performs its own ECC correction-algorithm.

Why is ECC error correction important?

Numerous analyzes and field-studies have proven DRAM single-bit errors to be the root cause of system-malfunctions or data-corruptions.

According to the field-study by the University Of Toronto called "DRAM Errors In The Wild – A Large-Scale field study", 25000 to 70000 ECC correctable single-bit errors occur per Megabit of DRAM within 1 billion hours of operation.

While not every single bit error causes a system crash, the application-software may become unstable or important data can be altered and the wrong data can pass through to external media, resulting in unrecoverable data-errors.

While all DRAMs are factory-tested by long burn-in-testing and effective functional and speed testing with different patterns and voltage variations, single-bit errors are technically not avoidable.

The effects are typically transient and difficult-to-repeat single data-bit flips. Many of these single-bit errors appear only under heavy stress or longer time of use of the DRAM, resulting as random system malfunctions or data-corruptions of the application. After a reset, the systems work again until the next occurrence of a single bit error reappears. It is difficult to prove a defect, as it is only a random effect which shows up in different ways at unknown times.

ECC corrects the output, but not the content of the Memory Array. For maximum stability we recommend to do periodical "scrubbing" (read and overwrite)

Possible root-causes for single-bit errors

DRAM cells consist of capacitors holding an electric charge which defines if the memory-cell contains a logical 0 or 1. These capacitor-cells are switched by transistors.With the trend to smaller process technologies, higher speeds and lower supply-voltages, DRAM memory cells become more sensitive to noise on the signals, electromagnetic fields, cosmic rays or particle radiation. Also power peaks and variations in the signal-timing can cause single-bit errors.

Furthermore, depending on the age and intensity of use of those DRAM components, memory-cells suffer from various degrees of degradation. The isolation of the capacitors gets reduced and leakage increases, leading to lower data-retention-times of some cells. As data-retention times approach the refresh-times, data-bit tend to sometimes show up an incorrect binary value. The effects often appear only with certain data-patterns, at specific temperatures or at high data-traffic to the DRAM. The cell gets "weak", but the errors in the cell are not easily repeatable as they are not permanent.

There is no way to improve the DRAM technology itself, except by going back to larger processes, lower speeds and higher voltages. Pre-Testing the DRAMs longer, with more stress and wider guard bands, or even with automotive certified screening-processes does not fully protect from the risk of single-bit errors.

The only practical way to avoid single-bit errors is to use error correction algorithms such as ECC.

Optional eXtra Robustness

Intelligent Memory ECC DRAMs are optionally available with an eXtra Robustness feature. To achieve additional robustness of the DRAM, two memory cells are being internally twinned so each two cells will together hold one bit. The total memory capacity is reduced by half, while at the same time the robustness against all above listed typical root-causes for single-bit errors gets heavily increased. In the rare case that even a twinned memory cell has a bit-flip, Intelligent Memory eXtra Robustness DRAM also has the ECC error correction functionality integrated which will correct the output data.

Table 1 - Ordering Information for RoHS Compliant Product				
Part Number	Module Density	Configuration	# of Ranks	Module Type
IMME256M64D3xSOD8AG-Ezzzy	2GB	256Mx64	2	2GB DDR3 Unbuffered SO-DIMM

Notes:
x: Operating Voltage
y: Operating Temperature
zzz: Speed Grade

Table 2 - Operating Voltage	
Part Number	Operating Voltage
Blank	VDD, VDDQ = 1.5V (1.425V-1.575V)

Table 3 - Temperature Grade		
Part Number	Temperature Grade	T_{case}
Blank	Commercial temperature	0°C to 95°C
I	Industrial temperature	-40°C to 95°C

Remark: Tcase is the case surface temperature on the center/top side of the DRAM. The refresh rate is required to double when 85 °C < Tcase <= 95 °C.

Table 4 - Speed Grade		
Part Number	Speed Grade	Max Clock Frequency (min. Clock Cycle time @ min. CAS Latency)
15E	PC3-10600 (DDR3-1333)	667MHz (1.5ns@CL=9)

Table 5 - Memory Chip Information					
Part Number	Base Device Brand	Base device	Voltage	Type	Chip Packing
IMME256M64D3SOD8AG-Ezzzy	I'M	IME1G08D3EEBG	1.5V	128Mx8	Lead Free

Part Number Decoder

IMME 256M64 D3 SO D 8 A G - E 15E (I)

Intelligent Memory Module by ECC DRAM

Module Configuration
256M64 = 256Mx64 (2GB)

Memory Type
D3 = DDR3

Module Form-Factor
SO = Unbuffered SO-DIMM

Number of Ranks
D = Dual Rank

Temperature Grade
Blank = Commercial Temperature (0°C to 95°C T_C)
I = Industrial Temperature (-40°C to 95°C T_C)

Speed Grade
15E = PC3-10600 / DDR3 1333

IC Revision
A = Revision A
B = Revision B
C = Revision C
E = Revision E

RoHS compliance
G = Green / RoHS

Module PCB Revision
A = Revision A
B = Revision B
C = Revision C

DRAM Bit width
8 = using x8 components

Table 6 - Addressing

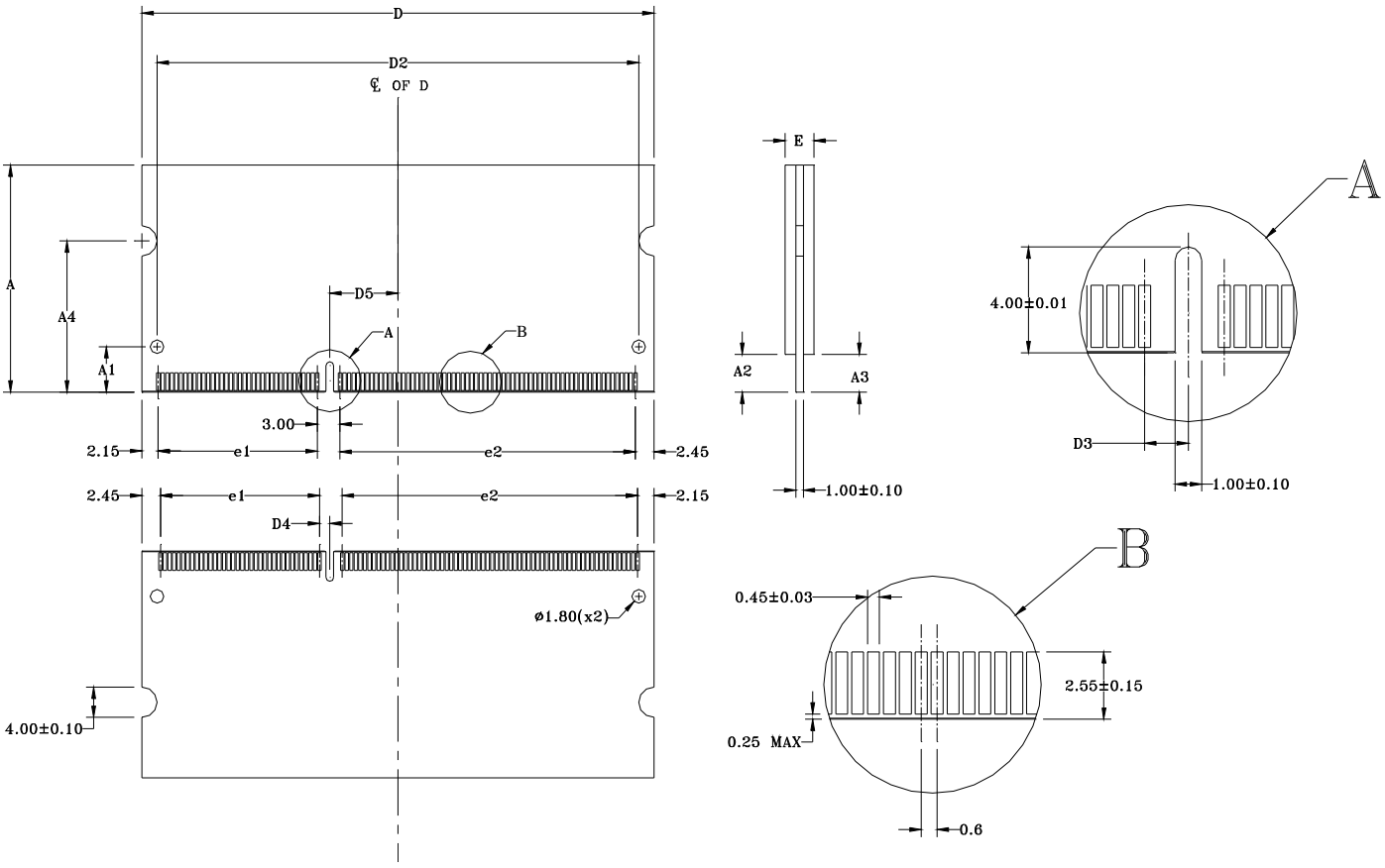
Parameter	2GB
Refresh count	8K
Row address	16K A[13:0]
Device bank address	8 BA[2:0]
Device configuration	1Gb (128Mx8)
Column address	1K A[9:0]
Module rank address	2 /S[1:0]
Number of devices	16

Table 7 - Pin Assignment

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VREFDQ	2	VSS	103	/CK0	104	/CK1
3	VSS	4	D4	105	VDD	106	VDD
5	D0	6	D5	107	A10, AP	108	BA1
7	D1	8	VSS	109	BA0	110	/RAS
9	VSS	10	/DQS0	111	VDD	112	VDD
11	DM0	12	DQS0	113	/WE	114	/S0
13	VSS	14	VSS	115	/CAS	116	ODT0
15	D2	16	D6	117	VDD	118	VDD
17	D3	18	D7	119	A13	120	ODT1
19	VSS	20	VSS	121	/S1	122	NC
21	D8	22	D12	123	VDD	124	VDD
23	D9	24	D13	125	NC	126	VREFCA
25	VSS	26	VSS	127	VSS	128	VSS
27	/DQS1	28	DM1	129	D32	130	D36
29	DQS1	30	/RESET	131	D33	132	D37
31	VSS	32	VSS	133	VSS	134	VSS
33	D10	34	D14	135	/DQS4	136	DM4
35	D11	36	D15	137	DQS4	138	VSS
37	VSS	38	VSS	139	VSS	140	D38
39	D16	40	D20	141	D34	142	D39
41	D17	42	D21	143	D35	144	VSS
43	VSS	44	VSS	145	VSS	146	D44
45	/DQS2	46	DM2	147	D40	148	D45
47	DQS2	48	VSS	149	D41	150	VSS
49	VSS	50	D22	151	VSS	152	/DQS5
51	D18	52	D23	153	DM5	154	DQS5
53	D19	54	VSS	155	VSS	156	VSS
55	VSS	56	D28	157	D42	158	D46
57	D24	58	D29	159	D43	160	D47
59	D25	60	VSS	161	VSS	162	VSS
61	VSS	62	/DQS3	163	D48	164	D52
63	DM3	64	DQS3	165	D49	166	D53
65	VSS	66	VSS	167	VSS	168	VSS
67	D26	68	D30	169	/DQS6	170	DM6
69	D27	70	D31	171	DQS6	172	VSS
71	VSS	72	VSS	173	VSS	174	D54
73	CKE0	74	CKE1	175	D50	176	D55
75	VDD	76	VDD	177	D51	178	VSS
77	NC	78	NC	179	VSS	180	D60
79	BA2	80	NC	181	D56	182	D61
81	VDD	82	VDD	183	D57	184	VSS
83	A12,/BC	84	A11	185	VSS	186	/DQS7
85	A9	86	A7	187	DM7	188	DQS7
87	VDD	88	VDD	189	VSS	190	VSS
89	A8	90	A6	191	D58	192	D62
91	A5	92	A4	193	D59	194	D63
93	VDD	94	VDD	195	VSS	196	VSS
95	A3	96	A2	197	SA0	198	NC
97	A1	98	A0	199	VDDSPD	200	SDA
99	VDD	100	VDD	201	SA1	202	SCL
101	CK0	102	CK1	203	VTT	204	VTT

Table 8 - Pin Description			
Pin Name	Description	Pin Name	Description
VDD	SDRAM core power supply	VREFDQ	SDRAM I/O reference supply
VREFCA	SDRAM command/address reference supply	VSS	Power supply return (ground)
A0-A13	SDRAM address bus	BA0-BA2	SDRAM bank addresses
CK0-CK1	SDRAM clocks (positive line of differential pair)	/CK0-/CK1	SDRAM clocks (negative line of differential pair)
/RAS	SDRAM row address strobe	/CAS	SDRAM column address strobe
/WE	SDRAM write enable	CKE0-CKE1	SDRAM clock enable lines
/S0-/S1	DIMM Rank Select Lines	ODT0-ODT1	On-die termination control lines
DQS0-DQS7	SDRAM data strobes (positive line of differential pair)	/DQS0-/DQS7	SDRAM data strobes (negative line of differential pair)
D0-D63	DIMM memory data bus	DM0-DM7	SDRAM data mask/high data strobes
NC	Spare Pins (no connect)	/RESET	Reset Pin
SCL	EEPROM clock	SDA	EEPROM date line
SA0-SA1	EEPROM address input	VDDSPD	EEPROM positive power supply
VTT	Termination Voltage		

Figure 1 – Module Dimension 204 Pin DDR3 SDRAM Unbuffered SO-DIMM



Symbol	MIN	NOM	MAX
A	29.85	30.00	30.15
A1		6.00 BSC	
A2	4.00		
A3	4.00		
A4		20.00 BSC	
D	67.45	67.60	67.75
D2		63.60 BSC	
D3		1.65 BSC	
D4		1.35 BSC	
D5		9.00 BSC	
e1		21.00 BSC	
e2		39.00 BSC	
E			3.80

Notes: 1. All dimensioning and tolerancing conform to ASME Y14.5M–1994.
2. Tolerances on all dimensions ± 0.15 unless otherwise specified.
3. All dimensions are in millimeters.