Product Specification | Rev. 1.0 | 2015

IMME128M64D3DUS8AG (Die Revision E)

1GByte (128M x 64 Bit)

1GB DDR3 Unbuffered DIMM
By ECC DRAM
RoHS Compliant Product

Version: Rev. 1.0, MAR 2015

1.0 - Initial release

Remark:
Please refer to the last page of the i) Contents ii) List of Table iii) List of Figures .

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Features

- 240-Pin Unbuffered Dual-In-Line Memory Module
- Capacity: 1GB
- JEDEC-Standard
- Built by ECC DRAM Chips
- Bi-directional Differential Data-Strobe
- 64 Bit Data Bus Width without ECC
- Programmable CAS Latency (CL):
  - PC3-10600: 5, 6, 7, 8, 9, 10
  - PC3-8500: 5, 6, 7, 8
- Programmable CAS Write Latency (CWL):
  - PC3-10600: 5, 6, 7
  - PC3-8500: 5, 6
- Programmable Additive Latency (Posted /CAS): 0, CL-2 or CL-1(Clock)
- On-Die Termination (ODT)
- ZQ Calibration Supported
- Burst Type (Sequential & Interleave)
- Burst Length: 4, 8
- Refresh Mode: Auto and Self
- 8192 Refresh Cycles / 64ms
- Asynchronous Reset
- Gold Edge Contacts
- 100% RoHS-Compliant
- Standard Module Height: 30.00mm (1.181 inch)

ECC DRAM Introduction

Special Features (ECC – Functionality)

- Embedded error correction code (ECC) functionality corrects single bit errors within each 64 bit memory-word.
- The error correction is performed automatically inside the ECC DRAM device.
- Parity data is generated by an internal ECC logic and then stored in additional, dedicated memory space
- Fully compatible to JEDEC standard DRAM operation and timings
- JEDEC compliant FBGA package (drop in replacement)

ECC – Functionality / Challenges and Achievements

During the production test, the ECC DRAMs are verified to pass extensive burn-in, core-function and speed tests throughout the complete memory array, including the memory-space for the parity-data. Only when every single memory cell has passed these tests, the ECC function is switched on by hardware and the products get shipped. With the ECC function activated, customers will have unparalleled functionality and quality.

Embedded ECC functionality

Intelligent Memory ECC DRAMs are JEDEC compliant components with integrated error-correction. The internal logic automatically detects and corrects single-bit-errors "on the fly" without any delays or additional latencies compared to conventional DRAM components. ECC DRAMs have additional memory-space to store the ECC-check-bits. Internally, the ECC DRAM works with a 72 bit wide buffer. When writing to the DRAM, an additional 8 ECC check-bits are being generated per each 64 bit data-word. Upon a Read-command, the whole 64+8 bit word is transferred to the buffer and automatically corrected by an ECC Hamming Code (72, 64). The corrected data is then applied to the DQ lines of the ECC DRAM in bit-widths of 4, 8, 16 or 32 bit, depending on the organization of the device.

The ECC algorithm is able to detect and correct one bit-error per 64+8 bit data-word. A 1 Gigabit ECC DRAM component has 16,777,216 data-words of 64 Bits. In each of these data-words, one single-bit error could be corrected, resulting in approximately 16 million times higher reliability of ECC DRAM compared to a conventional DRAM with similar capacity.

Note: If Burst Length x DRAM-I/O-width < 64 bit during a Write-command, the ECC-functionality is limited. Please contact Intelligent Memory for further details.

Comparison to conventional ECC implementation

ECC error correction is very common on high end industrial applications and servers. It normally requires an ECC-capable memory-controller which has an extra-wide data-bus with for example 72 bits (64 data-bits + 8 check-bits). The memory controller generates the required additional check-bits for the data and writes the extra wide data-word to the memory. Upon a Read-command, the memory controller will verify the data-integrity of the data-word + check-bits and performs the correction algorithm. Performing this algorithm affects the systems performance. In addition to the requirement for an ECC-capable memory controller, the conventional way of ECC correction requires multiple DRAMs to be accessed in parallel to achieve the extra-wide bit-width. On Server-memory-modules, for example, 18 DRAM-components with 4 data-lines each are put in parallel to reach the total 72 bit extra-wide data-bus.

With IM ECC DRAM, the check-bit-generation, verification and correction is performed inside the memory device. Every single ECC DRAM performs the error correction by itself, thus it does not require ECC-capable processors/controllers nor any wide data-bus between the controller and the DRAM. Because the ECC DRAM components are JEDEC compliant, they are drop-in replacements to conventional DRAM-memory. Any existing application that is currently built with conventional DRAM can be equipped with error-correction functionality. Note that, if a standard 64 bit memory-module is built using ECC DRAMs, the depth of error-correction is deeper than on 72 bit ECC memory module as each DRAM component on the module performs its own ECC correction-algorithm.

Why is ECC error correction important?

Numerous analyzes and field-studies have proven DRAM single-bit errors to be the root cause of system-malfunctions or data-corruptions.

According to the field-study by the University Of Toronto called "DRAM Errors In The Wild – A Large-Scale field study", 25000 to 70000 ECC correctable single-bit errors occur per Megabit of DRAM within 1 billion hours of operation.

While not every single bit error causes a system crash, the application-software may become unstable or important data can be altered and the wrong data can pass through to external media, resulting in unrecoverable data-errors.

While all DRAMs are factory-tested by long burn-in-testing and effective functional and speed testing with different patterns and voltage variations, single-bit errors are technically not avoidable.

The effects are typically transient and difficult-to-repeat single data-bit flips. Many of these single-bit errors appear only under heavy stress or longer time of use of the DRAM, resulting as random system malfunctions or data-corruptions of the application. After a reset, the systems work again until the next occurrence of a single bit error reappears. It is difficult to prove a defect, as it is only a random effect which shows up in different ways at unknown times.

ECC corrects the output, but not the content of the Memory Array. For maximum stability we recommend to do periodical "scrubbing" (read and overwrite)

Possible root-causes for single-bit errors

DRAM cells consist of capacitors holding an electric charge which defines if the memory-cell contains a logical 0 or 1. These capacitor-cells are switched by transistors.With the trend to smaller process technologies, higher speeds and lower supply-voltages, DRAM memory cells become more sensitive to noise on the signals, electromagnetic fields, cosmic rays or particle radiation. Also power peaks and variations in the signal-timing can cause single-bit errors.

Furthermore, depending on the age and intensity of use of those DRAM components, memory-cells suffer from various degrees of degradation. The isolation of the capacitors gets reduced and leakage increases, leading to lower data-retention-times of some cells. As data-retention times approach the refresh-times, data-bit tend to sometimes show up an incorrect binary value. The effects often appear only with certain data-patterns, at specific temperatures or at high data-traffic to the DRAM. The cell gets "weak", but the errors in the cell are not easily repeatable as they are not permanent.

There is no way to improve the DRAM technology itself, except by going back to larger processes, lower speeds and higher voltages. Pre-Testing the DRAMs longer, with more stress and wider guard bands, or even with automotive certified screening-processes does not fully protect from the risk of single-bit errors.

The only practical way to avoid single-bit errors is to use error correction algorithms such as ECC.

Optional eXtra Robustness

Intelligent Memory ECC DRAMs are optionally available with an eXtra Robustness feature. To achieve additional robustness of the DRAM, two memory cells are being internally twinned so each two cells will together hold one bit. The total memory capacity is reduced by half, while at the same time the robustness against all above listed typical root-causes for single-bit errors gets heavily increased. In the rare case that even a twinned memory cell has a bit-flip, Intelligent Memory eXtra Robustness DRAM also has the ECC error correction functionality integrated which will correct the output data.

Table 1 - Ordering Information for RoHS Compliant Product				
Part Number	Module Density	Configuration	# of Ranks	Module Type
IMME128M64D3xDUS8AG-Ezzzy	1GB	128Mx64	1	1GB DDR3 Unbuffered DIMM

Notes:
x: Operating Voltage
y: Operating Temperature
zzz: Speed Grade

Table 2 - Operating Voltage	
Part Number	Operating Voltage
Blank	VDD, VDDQ = 1.5V (1.425V-1.575V)

Table 3 - Temperature Grade		
Part Number	Temperature Grade	T_{case}
Blank	Commercial temperature	0°C to 95°C
I	Industrial temperature	-40°C to 95°C

Remark: Tcase is the case surface temperature on the center/top side of the DRAM. The refresh rate is required to double when 85 °C < Tcase <= 95 °C.

Table 4 - Speed Grade		
Part Number	Speed Grade	Max Clock Frequency (min. Clock Cycle time @ min. CAS Latency)
15E	PC3-10600 (DDR3-1333)	667MHz (1.5ns@CL=9)
187E	PC3-8500 (DDR3-1066)	533MHz (1.87ns@CL=7)

Table 5 - Memory Chip Information					
Part Number	Base Device Brand	Base Device	Voltage	Type	Chip Packing
IMME128M64D3DUS8AG-Ezzzy	I'M	IME1G08D3EEBG	1.5V	128Mx8	Lead Free

Part Number Decoder

IMME 128M64 D3 (L) DU S 8 A G - E 15E (I)

Intelligent Memory Module by ECC DRAM

Module Configuration
128M64 = 128Mx64 (1GB)

Memory Type
D3 = DDR3

DDR3L option
Blank = 1.5 Volt

Module Form-Factor
DU = Unbuffered DIMM

Number of Ranks
S = Single Rank

Temperature Grade
Blank = Commercial Temperature (0°C to 95°C T_C)
I = Industrial Temperature (-40°C to 95°C T_C)

Speed Grade
187E = PC3-8500 / DDR3 1066
15E = PC3-10600 / DDR3 1333

IC Revision
A = Revision A
B = Revision B
C = Revision C
E = Revision E

RoHS compliance
G = Green / RoHS

Module PCB Revision
A = Revision A
B = Revision B
C = Revision C

DRAM Bit width
8 = using x8 components

Table 6 - Addressing

Parameter	1GB
Refresh count	8K
Row address	16K A[13:0]
Device bank address	8 BA[2:0]
Device configuration	1Gb (128Mx8)
Column address	1K A[9:0]
Module rank address	1 /S[0]
Number of devices	8

Table 7 - Pin Assignment

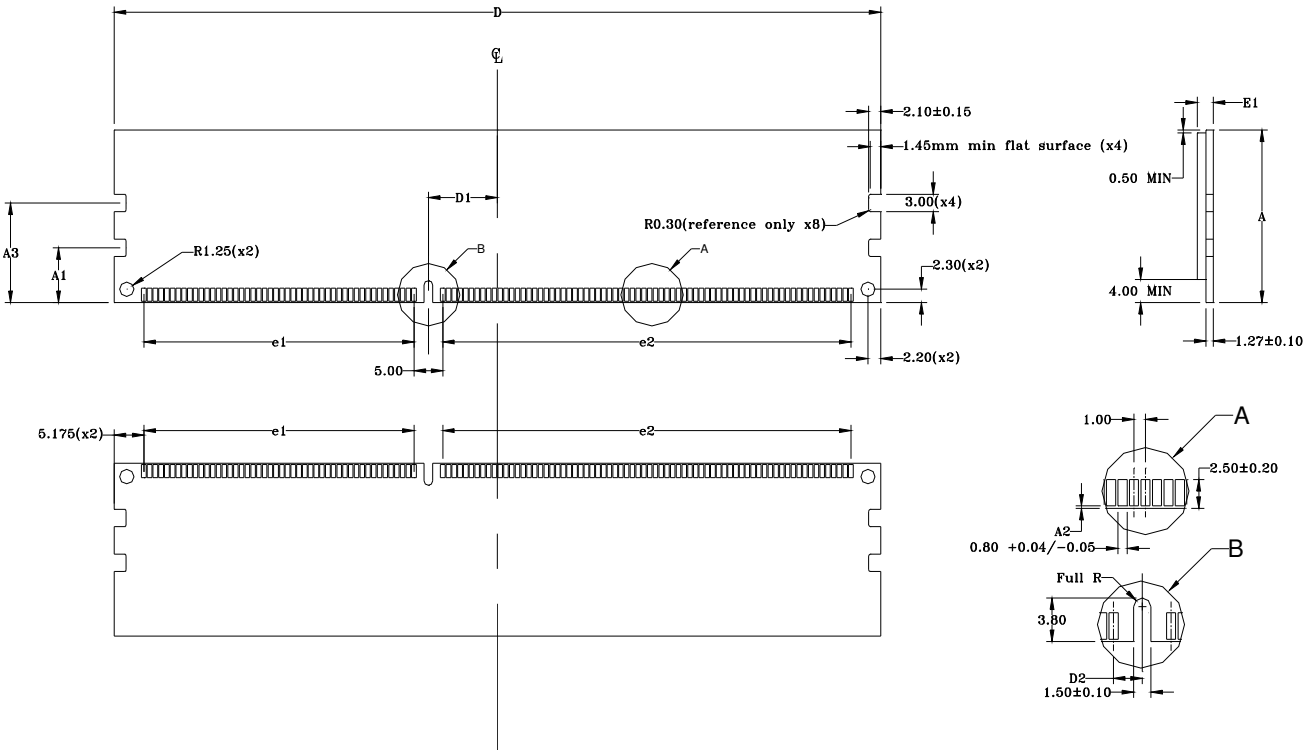
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VREFDQ	121	VSS	61	A2	181	A1
2	VSS	122	D4	62	VDD	182	VDD
3	D0	123	D5	63	CK1	183	VDD
4	D1	124	VSS	64	/CK1	184	CK0
5	VSS	125	DM0	65	VDD	185	/CK0
6	/DQS0	126	NC	66	VDD	186	VDD
7	DQS0	127	VSS	67	VREFCA	187	NC
8	VSS	128	D6	68	NC	188	A0
9	D2	129	D7	69	VDD	189	VDD
10	D3	130	VSS	70	A10, AP	190	BA1
11	VSS	131	D12	71	BA0	191	VDD
12	D8	132	D13	72	VDD	192	/RAS
13	D9	133	VSS	73	/WE	193	/S0
14	VSS	134	DM1	74	/CAS	194	VDD
15	/DQS1	135	NC	75	VDD	195	ODT0
16	DQS1	136	VSS	76	NC	196	A13
17	VSS	137	D14	77	NC	197	VDD
18	D10	138	D15	78	VDD	198	NC
19	D11	139	VSS	79	NC	199	VSS
20	VSS	140	D20	80	VSS	200	D36
21	D16	141	D21	81	D32	201	D37
22	D17	142	VSS	82	D33	202	VSS
23	VSS	143	DM2	83	VSS	203	DM4
24	/DQS2	144	NC	84	/DQS4	204	NC
25	DQS2	145	VSS	85	DQS4	205	VSS
26	VSS	146	D22	86	VSS	206	D38
27	D18	147	D23	87	D34	207	D39
28	D19	148	VSS	88	D35	208	VSS
29	VSS	149	D28	89	VSS	209	D44
30	D24	150	D29	90	D40	210	D45
31	D25	151	VSS	91	D41	211	VSS
32	VSS	152	DM3	92	VSS	212	DM5
33	/DQS3	153	NC	93	/DQS5	213	NC
34	DQS3	154	VSS	94	DQS5	214	VSS
35	VSS	155	D30	95	VSS	215	D46
36	D26	156	D31	96	D42	216	D47
37	D27	157	VSS	97	D43	217	VSS
38	VSS	158	NC	98	VSS	218	D52
39	NC	159	NC	99	D48	219	D53
40	NC	160	VSS	100	D49	220	VSS
41	VSS	161	NC	101	VSS	221	DM6
42	NC	162	NC	102	/DQS6	222	NC
43	NC	163	VSS	103	DQS6	223	VSS
44	VSS	164	NC	104	VSS	224	D54
45	NC	165	NC	105	D50	225	D55
46	NC	166	VSS	106	D51	226	VSS
47	VSS	167	NC	107	VSS	227	D60
48	NC	168	/RESET	108	D56	228	D61
49	NC	169	NC	109	D57	229	VSS
50	CKE0	170	VDD	110	VSS	230	DM7
51	VDD	171	NC	111	/DQS7	231	NC
52	BA2	172	NC	112	DQS7	232	VSS
53	NC	173	VDD	113	VSS	233	D62
54	VDD	174	A12, /BC	114	D58	234	D63
55	A11	175	A9	115	D59	235	VSS
56	A7	176	VDD	116	VSS	236	VDDSPD
57	VDD	177	A8	117	SA0	237	SA1
58	A5	178	A6	118	SCL	238	SDA

Pin	Name	Pin	Name	Pin	Name	Pin	Name
59	A4	179	VDD	119	SA2	239	VSS
60	VDD	180	A3	120	VTT	240	VTT

Table 8 - Pin Description

Pin Name	Description	Pin Name	Description
VDD	SDRAM core power supply	VREFDQ	SDRAM I/O reference supply
VREFCA	SDRAM command/address reference supply	VSS	Power supply return (ground)
A0-A13	SDRAM address bus	BA0-BA2	SDRAM bank addresses
CK0-CK1	SDRAM clocks (positive line of differential pair)	/CK0-/CK1	SDRAM clocks (negative line of differential pair)
/RAS	SDRAM row address strobe	/CAS	SDRAM column address strobe
/WE	SDRAM write enable	CKE0	SDRAM clock enable lines
/S0	DIMM Rank Select Lines	ODT0	On-die termination control lines
DQS0-DQS7	SDRAM data strobes (positive line of differential pair)	/DQS0-/DQS7	SDRAM data strobes (negative line of differential pair)
D0-D63	DIMM memory data bus	DM0-DM7	SDRAM data mask/high data strobes
SCL	EEPROM clock	SDA	EEPROM date line
SA0-SA1	EEPROM address input	VDDSPD	EEPROM positive power supply
/RESET	Reset Pin	VTT	Termination Voltage
NC	Spare Pins (no connect)		

Figure 1 – Module Dimension 240 Pin DDR3 SDRAM Unbuffered DIMM



Symbol	MIN	NOM	MAX
A	29.85	30.00	30.50
A1	9.35	9.50	9.65
A2	0.05	0.20	0.35
A3	17.15	17.30	17.45
D	133.20	133.35	133.50
D1		12.00BSC	
D2		2.50BSC	
e1		47.00BSC	
e2		71.00BSC	
E1			2.70

Notes:

1 All dimensioning and tolerancing conform to ASME Y14.5M–1994.
2 Tolerance on all dimensions ± 0.15 unless otherwise specified.
3 All dimensions are in millimeters.