Product Specification | Rev. 1.0 | 2015

IMME128M64D2DUS8AG (Die Revision E)

1GByte (128M x 64 Bit)

1GB DDR2 Unbuffered DIMM
By ECC DRAM
RoHS Compliant Product

Version: Rev. 1.0, MAR 2015

1.0 - Initial release

Remark:
Please refer to the last page of the i) Contents ii) List of Table iii) List of Figures .

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Features

- 200-Pin Unbuffered Small Outline Dual-In-Line Memory Module
- Capacity: 1GB
- Maximum Data Transfer Rate: 6.40 GB/Sec
- JEDEC-Standard
- Built by ECC DRAM Chips
- Power Supply: VDD, VDDQ =1.8± 0.1 V
- Bi-directional Differential Data-Strobe (Single-ended data-strobe is an optional feature)
- 64 Bit Data Bus Width without ECC
- Programmable CAS Latency (CL):
    - PC2-6400: 4, 5, 6
    - PC2-5300: 4, 5
- Programmable Additive Latency (Posted /CAS) : 0, CL-2 or CL-1(Clock)
- Write Latency (WL) = Read Latency (RL) -1
- Posted /CAS
- On-Die Termination (ODT)
- Off-Chip Driver (OCD) Impedance Adjustment
- Burst Type (Sequential & Interleave)
- Burst Length: 4, 8
- Refresh Mode: Auto and Self
- 8192 Refresh Cycles / 64ms
- Serial Presence Detect (SPD) with EEPROM
- SSTL_18 Interface
- Gold Edge Contacts
- 100% RoHS-Compliant
- Standard Module Height: 30.00mm (1.18 inch)

ECC DRAM Introduction

Special Features (ECC – Functionality)

- Embedded error correction code (ECC) functionality corrects single bit errors within each 64 bit memory-word.
- The error correction is performed automatically inside the ECC DRAM device.
- Parity data is generated by an internal ECC logic and then stored in additional, dedicated memory space
- Fully compatible to JEDEC standard DRAM operation and timings
- JEDEC compliant FBGA package (drop in replacement)

ECC – Functionality / Challenges and Achievements

During the production test, the ECC DRAMs are verified to pass extensive burn-in, core-function and speed tests throughout the complete memory array, including the memory-space for the parity-data. Only when every single memory cell has passed these tests, the ECC function is switched on by hardware and the products get shipped. With the ECC function activated, customers will have unparalleled functionality and quality.

Embedded ECC functionality

Intelligent Memory ECC DRAMs are JEDEC compliant components with integrated error-correction. The internal logic automatically detects and corrects single-bit-errors "on the fly" without any delays or additional latencies compared to conventional DRAM components. ECC DRAMs have additional memory-space to store the ECC-check-bits. Internally, the ECC DRAM works with a 72 bit wide buffer. When writing to the DRAM, an additional 8 ECC check-bits are being generated per each 64 bit data-word. Upon a Read-command, the whole 64+8 bit word is transferred to the buffer and automatically corrected by an ECC Hamming Code (72, 64). The corrected data is then applied to the DQ lines of the ECC DRAM in bit-widths of 4, 8, 16 or 32 bit, depending on the organization of the device.

The ECC algorithm is able to detect and correct one bit-error per 64+8 bit data-word. A 1 Gigabit ECC DRAM component has 16,777,216 data-words of 64 Bits. In each of these data-words, one single-bit error could be corrected, resulting in approximately 16 million times higher reliability of ECC DRAM compared to a conventional DRAM with similar capacity.

Note: If Burst Length x DRAM-I/O-width < 64 bit during a Write-command, the ECC-functionality is limited. Please contact Intelligent Memory for further details.

Comparison to conventional ECC implementation

ECC error correction is very common on high end industrial applications and servers. It normally requires an ECC-capable memory-controller which has an extra-wide data-bus with for example 72 bits (64 data-bits + 8 check-bits). The memory controller generates the required additional check-bits for the data and writes the extra wide data-word to the memory. Upon a Read-command, the memory controller will verify the data-integrity of the data-word + check-bits and performs the correction algorithm. Performing this algorithm affects the systems performance. In addition to the requirement for an ECC-capable memory controller, the conventional way of ECC correction requires multiple DRAMs to be accessed in parallel to achieve the extra-wide bit-width. On Server-memory-modules, for example, 18 DRAM-components with 4 data-lines each are put in parallel to reach the total 72 bit extra-wide data-bus.

With IM ECC DRAM, the check-bit-generation, verification and correction is performed inside the memory device. Every single ECC DRAM performs the error correction by itself, thus it does not require ECC-capable processors/controllers nor any wide data-bus between the controller and the DRAM. Because the ECC DRAM components are JEDEC compliant, they are drop-in replacements to conventional DRAM-memory. Any existing application that is currently built with conventional DRAM can be equipped with error-correction functionality. Note that, if a standard 64 bit memory-module is built using ECC DRAMs, the depth of error-correction is deeper than on 72 bit ECC memory module as each DRAM component on the module performs its own ECC correction-algorithm.

Why is ECC error correction important?

Numerous analyzes and field-studies have proven DRAM single-bit errors to be the root cause of system-malfunctions or data-corruptions.

According to the field-study by the University Of Toronto called "DRAM Errors In The Wild – A Large-Scale field study", 25000 to 70000 ECC correctable single-bit errors occur per Megabit of DRAM within 1 billion hours of operation.

While not every single bit error causes a system crash, the application-software may become unstable or important data can be altered and the wrong data can pass through to external media, resulting in unrecoverable data-errors.

While all DRAMs are factory-tested by long burn-in-testing and effective functional and speed testing with different patterns and voltage variations, single-bit errors are technically not avoidable.

The effects are typically transient and difficult-to-repeat single data-bit flips. Many of these single-bit errors appear only under heavy stress or longer time of use of the DRAM, resulting as random system malfunctions or data-corruptions of the application. After a reset, the systems work again until the next occurrence of a single bit error reappears. It is difficult to prove a defect, as it is only a random effect which shows up in different ways at unknown times.

ECC corrects the output, but not the content of the Memory Array. For maximum stability we recommend to do periodical "scrubbing" (read and overwrite)

Possible root-causes for single-bit errors

DRAM cells consist of capacitors holding an electric charge which defines if the memory-cell contains a logical 0 or 1. These capacitor-cells are switched by transistors.With the trend to smaller process technologies, higher speeds and lower supply-voltages, DRAM memory cells become more sensitive to noise on the signals, electromagnetic fields, cosmic rays or particle radiation. Also power peaks and variations in the signal-timing can cause single-bit errors.

Furthermore, depending on the age and intensity of use of those DRAM components, memory-cells suffer from various degrees of degradation. The isolation of the capacitors gets reduced and leakage increases, leading to lower data-retention-times of some cells. As data-retention times approach the refresh-times, data-bit tend to sometimes show up an incorrect binary value. The effects often appear only with certain data-patterns, at specific temperatures or at high data-traffic to the DRAM. The cell gets "weak", but the errors in the cell are not easily repeatable as they are not permanent.

There is no way to improve the DRAM technology itself, except by going back to larger processes, lower speeds and higher voltages. Pre-Testing the DRAMs longer, with more stress and wider guard bands, or even with automotive certified screening-processes does not fully protect from the risk of single-bit errors.

The only practical way to avoid single-bit errors is to use error correction algorithms such as ECC.

Optional eXtra Robustness

Intelligent Memory ECC DRAMs are optionally available with an eXtra Robustness feature. To achieve additional robustness of the DRAM, two memory cells are being internally twinned so each two cells will together hold one bit. The total memory capacity is reduced by half, while at the same time the robustness against all above listed typical root-causes for single-bit errors gets heavily increased. In the rare case that even a twinned memory cell has a bit-flip, Intelligent Memory eXtra Robustness DRAM also has the ECC error correction functionality integrated which will correct the output data.

Table 1 - Ordering Information for RoHS Compliant Product				
Part Number	Module Density	Configuration	# of Ranks	Module Type
IMME128M64D2DUS8AG-Ezzzy	1GB	128Mx64	1	1GB DDR2 Unbuffered DIMM

Notes:
y: Operating Temperature
zzz: Speed Grade

Table 2 - Temperature Grade		
Part Number	Temperature Grade	T_{case}
Blank	Commercial temperature	0°C to 85°C
I	Industrial temperature	-40°C to 95°C

Remark: Tcase is the case surface temperature on the center/top side of the DRAM. The refresh rate is required to double when 85 °C < Tcase <= 95 °C.

Table 3 - Speed Grade		
Part Number	Speed Grade	Max Clock Frequency (min. Clock Cycle time @ min. CAS Latency)
25	PC2-6400 (DDR2-800)	400MHz (2.5ns@CL=6)
3	PC2-5300 (DDR2-667)	333MHz (3.0ns@CL=5)

Table 4 - Memory Chip Information					
Part Number	Base Device Brand	Base device	Voltage	Type	Chip Packing
IMME128M64D2DUS8AG-Ezzzy	I'M	IME1G08D2DEBG	1.8V	128Mx8	Lead Free

Part Number Decoder

IMME 128M64 D2 DU S 8 A G - E 25 I

Intelligent Memory Module by ECC DRAM

Module Configuration
128M64 = 128Mx64 (1GB)

Memory Type
D2 = DDR2

Module Form-Factor
DU = Unbuffered SO-DIMM

Number of Ranks
S = Single Rank

DRAM Bit width
8 = using x8 components

Module PCB Revision
A = Revision A
B = Revision B
C = Revision C

RoHS compliance
G = Green / RoHS

IC Revision
A = Revision A
B = Revision B
C = Revision C
E = Revision E

Speed Grade
3 = PC2-5300 / DDR2-667
25 = PC2-6400 / DDR2-800

Temperature Grade
Blank = Commercial Temperature (0°C to 85°C T_C)
I = Industrial Temperature (-40°C to 95°C T_C)

Table 5 - Addressing

Parameter	1GB
Refresh count	8K
Row address	16K A[13:0]
Device bank address	8 BA[2:0]
Device configuration	1Gb (128Mx8)
Column address	1K A[9:0]
Module rank address	1 /S[0]
Number of devices	8

Table 2 - Pin Assignment

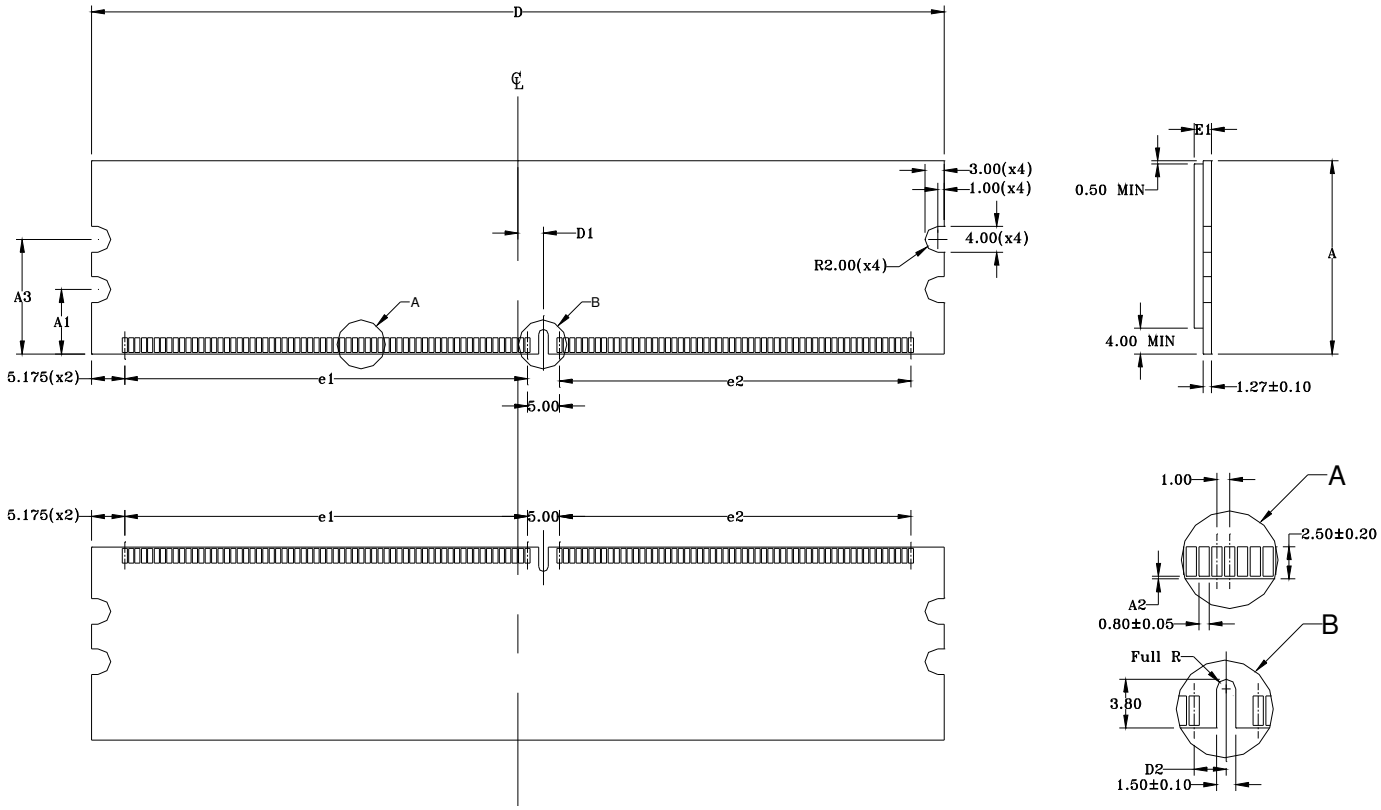
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VREF	121	VSS	61	A4	181	VDDQ
2	VSS	122	D4	62	VDDQ	182	A3
3	D0	123	D5	63	A2	183	A1
4	D1	124	VSS	64	VDD	184	VDD
5	VSS	125	DM0	65	VSS	185	CK0
6	/DQS0	126	NC	66	VSS	186	/CK0
7	DQS0	127	VSS	67	VDD	187	VDD
8	VSS	128	D6	68	NC	188	A0
9	D2	129	D7	69	VDD	189	VDD
10	D3	130	VSS	70	A10, AP	190	BA1
11	VSS	131	D12	71	BA0	191	VDDQ
12	D8	132	D13	72	VDDQ	192	/RAS
13	D9	133	VSS	73	/WE	193	/S0
14	VSS	134	DM1	74	/CAS	194	VDDQ
15	/DQS1	135	NC	75	VDDQ	195	ODT0
16	DQS1	136	VSS	76	/S1	196	A13
17	VSS	137	CK1	77	ODT1	197	VDD
18	NC	138	/CK1	78	VDDQ	198	VSS
19	NC	139	VSS	79	VSS	199	D36
20	VSS	140	D14	80	D32	200	D37
21	D10	141	D15	81	D33	201	VSS
22	D11	142	VSS	82	VSS	202	DM4
23	VSS	143	D20	83	/DQS4	203	NC
24	D16	144	D21	84	DQS4	204	VSS
25	D17	145	VSS	85	VSS	205	D38
26	VSS	146	DM2	86	D34	206	D39
27	/DQS2	147	NC	87	D35	207	VSS
28	DQS2	148	VSS	88	VSS	208	D44
29	VSS	149	D22	89	D40	209	D45
30	D18	150	D23	90	D41	210	VSS
31	D19	151	VSS	91	VSS	211	DM5
32	VSS	152	D28	92	/DQS5	212	NC
33	D24	153	D29	93	DQS5	213	VSS
34	D25	154	VSS	94	VSS	214	D46
35	VSS	155	DM3	95	D42	215	D47
36	/DQS3	156	NC	96	D43	216	VSS
37	DQS3	157	VSS	97	VSS	217	D52
38	VSS	158	D30	98	D48	218	D53
39	D26	159	D31	99	D49	219	VSS
40	D27	160	VSS	100	VSS	220	NC
41	VSS	161	NC	101	SA2	221	NC
42	NC	162	NC	102	NC	222	VSS
43	NC	163	VSS	103	VSS	223	DM6
44	VSS	164	NC	104	/DQS6	224	NC
45	NC	165	NC	105	DQS6	225	VSS
46	NC	166	VSS	106	VSS	226	D54
47	VSS	167	NC	107	D50	227	D55
48	NC	168	NC	108	D51	228	VSS
49	NC	169	VSS	109	VSS	229	D60
50	VSS	170	VDDQ	110	D56	230	D61
51	VDDQ	171	NC	111	D57	231	VSS
52	CKE0	172	VDD	112	VSS	232	DM7
53	VDD	173	NC	113	/DQS7	233	NC
54	BA2	174	NC	114	DQS7	234	VSS
55	NC	175	VDDQ	115	VSS	235	D62
56	VDDQ	176	A12	116	D58	236	D63
57	A11	177	A9	117	D59	237	VSS
58	A7	178	VDD	118	VSS	238	VDDSPD

Pin	Name	Pin	Name	Pin	Name	Pin	Name
59	VDD	179	A8	119	SDA	239	SA0
60	A5	180	A6	120	SCL	240	SA1

Table 7 - Pin Description

Pin Name	Description	Pin Name	Description
VDD	SDRAM core power supply	VREFDQ	SDRAM I/O reference supply
VREFCA	SDRAM command/address reference supply	VSS	Power supply return (ground)
A0-A13	SDRAM address bus	BA0-BA2	SDRAM bank addresses
CK0-CK1	SDRAM clocks (positive line of differential pair)	/CK0-/CK1	SDRAM clocks (negative line of differential pair)
/RAS	SDRAM row address strobe	/CAS	SDRAM column address strobe
/WE	SDRAM write enable	CKE0	SDRAM clock enable lines
/S0	DIMM Rank Select Lines	ODT0	On-die termination control lines
DQS0-DQS7	SDRAM data strobes (positive line of differential pair)	/DQS0-/DQS7	SDRAM data strobes (negative line of differential pair)
D0-D63	DIMM memory data bus	DM0-DM7	SDRAM data mask/high data strobes
SCL	EEPROM clock	/RESET	Reset Pin
SA0-SA1	EEPROM address input	SDA	EEPROM date line
VTT	Termination Voltage	VDDSPD	EEPROM positive power supply
NC	Spare Pins (no connect)		

Figure 1 – Module Dimension 240 Pin DDR2 SDRAM Unbuffered DIMM



Symbol	MIN	NOM	MAX
A	29.85	30.00	30.50
A1		10.00 Basic	
A2	0.05	0.20	0.35
A3		17.80 Basic	
D	133.20	133.35	133.50
D1		4.00 Basic	
D2		2.50 Basic	
e1		63.00 Basic	
e2		55.00 Basic	
E1			2.70

Notes:

1. Dimensioning and tolerancing conform to ASME Y14.5M–1994.
2. Tolerances on all dimensions ± 0.15 unless otherwise specified.
3. All dimensions are in millimeters.