Product Specification | Rev. 1.0 | 2015

IMM64M72D1DVS8AG (Die Revision F)
512MByte (64M x 72 Bit)

512MB DDR ECC VLP Unbuffered DIMM
RoHS Compliant Product

Version: Rev. 1.0, JUN 2015

1.0 - Initial release

Remark:
Please refer to the last page of the i) Contents ii) List of Table iii) List of Figures .

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Features

- 184-Pin Unbuffered Dual-In-Line Memory Module
- Capacity: 512MB
- Power Supply:
  DDR 400: VDD, VDDQ = 2.6± 0.1 V
  DDR 333, 266: VDD, VDDQ = 2.5± 0.2 V
- Two Data Transfer per Clock Cycle
- Differential Clock Input (CK and /CK)
- 72 Bit Data Bus Width with ECC
- Programmable CAS Latency (CL):
  - PC-3200: 2.5, 3
  - PC-2700: 2.5
- Burst Type (Sequential & Interleave)
- Burst Length: 2, 4, 8
- Refresh Mode: Auto and Self
- 8192 Refresh Cycles / 64ms
- Serial Presence Detect (SPD) with EEPROM
- Double Sided Components
- 100% RoHS-Compliant
- Gold Edge Contacts
- Very Low Profile Module Height: 25.40mm (1.00 inch)

Table 1 - Ordering Information for RoHS Compliant Product				
Part Number	Module Density	Configuration	# of Ranks	Module Type
IMM64M72D1DVS8AG-Fzzzy	512MB	64Mx72	1	512M DDR ECC VLP Unbuffered DIMM

Notes:
y: Operating Temperature
zzz: Speed Grade

Table 2 - Temperature Grade		
Part Number	Temperature Grade	T_a
Blank	Commercial temperature	0°C to 70°C
I	Industrial temperature	-40°C to 85°C

Table 3 - Speed Grade		
Part Number	Speed Grade	Max Clock Frequency (min. Clock Cycle time @ min. CAS Latency)
5	PC3200	200MHz (5.0ns@CL=3)
6	PC2700	166MHz (6.0ns@CL=2.5)

Table 4 - Memory Chip Information					
Part Number	Base Device Brand	Base Device	Voltage	Type	Chip Packing
IMM64M72D1DVS8AG-Fzzzy	I'M	IM5108D1CFBG	2.5V	64Mx8	Lead Free

Part Number Decoder

IMM 64M72 D1 DV S 8 A G - F 5 (I)

Intelligent Memory Module

Module Configuration
64M72 = 64Mx72 (512MB)

Memory Type
D1 = DDR

Module Form-Factor
DV = VLP Unbuffered DIMM

Number of Ranks
S = Single Rank

DRAM Bit width
8 = using x8 components

Module PCB Revision
A = Revision A
B = Revision B
C = Revision C

RoHS compliance
G = Green / RoHS

IC Revision
F = Revision F

Speed Grade
6 = PC-2700 / DDR-333
5 = PC-3200 / DDR-400

Temperature Grade
Blank = Commercial Temperature (0°C to 70°C T_a)
I = Industrial Temperature (-40°C to 85°C T_a)

Table 5 – Addressing

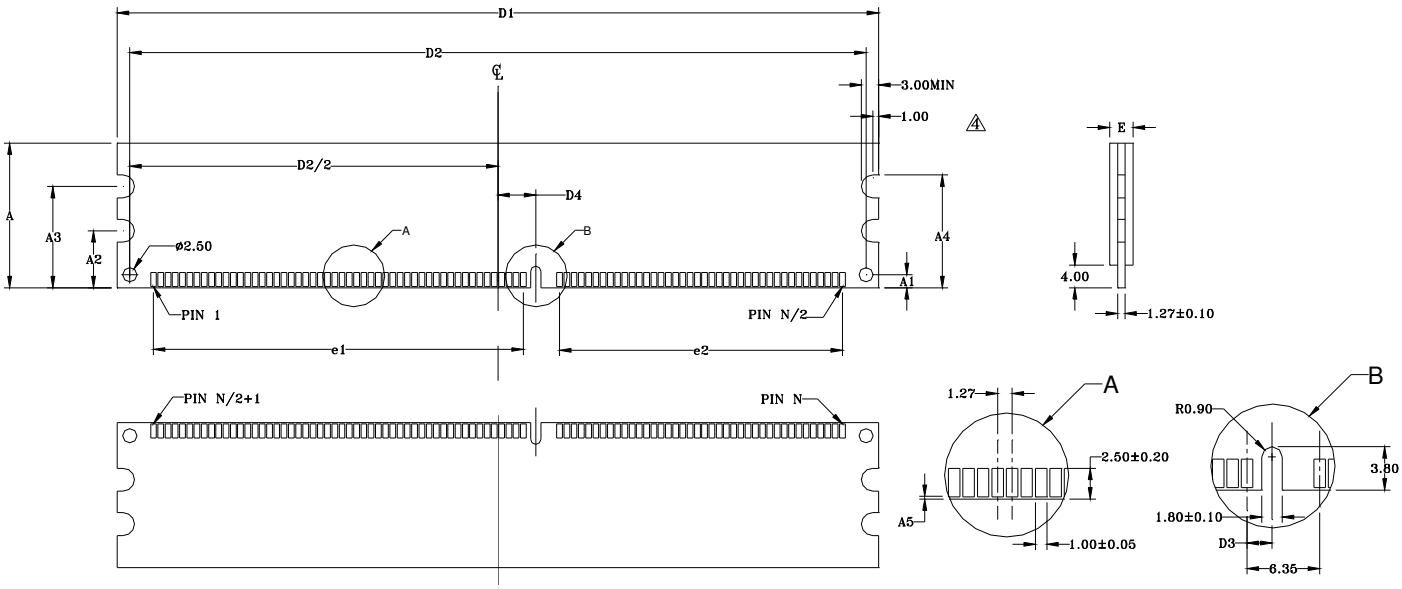
Parameter	512MB
Refresh count	8K
Row address	8K A[12:0]
Device bank address	4 BA[1:0]
Device configuration	512Mb (64Mx8)
Column address	2K A[9:0], A11
Module rank address	1 /S[0]
Number of devices	9

Table 6 - Pin Assignment

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VREF	47	DQS8	93	VSS	139	VSS
2	D0	48	A0	94	D4	140	DM8, DQS17
3	VSS	49	CB2	95	D5	141	A10, AP
4	D1	50	VSS	96	VDDQ	142	CB6
5	DQS0	51	CB3	97	DM0, DQS9	143	VDDQ
6	D2	52	BA1	98	D6	144	CB7
7	VDD	53	D32	99	D7	145	VSS
8	D3	54	VDDQ	100	VSS	146	D36
9	NC	55	D33	101	NC	147	D37
10	NC	56	DQS4	102	NC	148	VDD
11	VSS	57	D34	103	NC	149	DM4, DQS13
12	D8	58	VSS	104	VDDQ	150	D38
13	D9	59	BA0	105	D12	151	D39
14	DQS1	60	D35	106	D13	152	VSS
15	VDDQ	61	D40	107	DM1, DQS10	153	D44
16	CK1	62	VDDQ	108	VDD	154	/RAS
17	/CK1	63	/WE	109	D14	155	D45
18	VSS	64	D41	110	D15	156	VDDQ
19	D10	65	/CAS	111	NC	157	/S0
20	D11	66	VSS	112	VDDQ	158	NC
21	CKE0	67	DQS5	113	NC	159	DM5, DQS14
22	VDDQ	68	D42	114	D20	160	VSS
23	D16	69	D43	115	A12	161	D46
24	D17	70	VDD	116	VSS	162	D47
25	DQS2	71	NC	117	D21	163	NC
26	VSS	72	D48	118	A11	164	VDDQ
27	A9	73	D49	119	DM2, DQS11	165	D52
28	D18	74	VSS	120	VDD	166	D53
29	A7	75	/CK2	121	D22	167	NC
30	VDDQ	76	CK2	122	A8	168	VDD
31	D19	77	VDDQ	123	D23	169	DM6, DQS15
32	A5	78	DQS6	124	VSS	170	D54
33	D24	79	D50	125	A6	171	D55
34	VSS	80	D51	126	D28	172	VDDQ
35	D25	81	VSS	127	D29	173	NC
36	DQS3	82	VDDID	128	VDDQ	174	D60
37	A4	83	D56	129	DM3, DQS12	175	D61
38	VDD	84	D57	130	A3	176	VSS
39	D26	85	VDD	131	D30	177	DM7, DQS16
40	D27	86	DQS7	132	VSS	178	D62
41	A2	87	D58	133	D31	179	D63
42	VSS	88	D59	134	CB4	180	VDDQ
43	A1	89	VSS	135	CB5	181	SA0
44	CB0	90	NC	136	VDDQ	182	SA1
45	CB1	91	SDA	137	CK0	183	SA2
46	VDD	92	SCL	138	/CK0	184	VDDSPD

Table 7 - Pin Description			
Pin Name	Description	Pin Name	Description
VDD	SDRAM positive power supply	VSS	Power supply return (ground)
VREF	Input or Output reference supply	VDDQ	SDRAM input or output driver positive power supply
VDDSPD	EEPROM power	VDDID	Voltage identification flag
CK0-CK2	Clock Input (Positive)	/CK0-/CK2	Clock Input (Negative)
A0-A12	Address Input	BA0-BA1	SDRAM Bank Address
D0-D63	DIMM memory data bus	/S0	Chip selects
DQS0-DQS8	Data Strobe	DM0-DM8, DQS9-DQS17	SDRAM Data Mask
CB0-CB7	Data check bits input/output	CKE0	Clock Enable
/WE	Write Enable	/CAS	Column address strobe
/RAS	Row address strobe	SCL	EEPROM Clock Input
SDA	EEPROM Data Input or Output	SA0-SA2	EEPROM slave address select
NC	Spare Pin (no connect)		

Figure 1 –Module Dimension 184 Pin DDR SDRAM VLP Unbuffered DIMM



Symbol	MIN	NOM	MAX
A	25.25	25.40	25.55
A1		2.30 BSC	
A2		10.00 BSC	
A3		17.80 BSC	
A4		19.80 BSC	
A5	0.05	0.20	0.35
D1	133.20	133.35	133.50
D2		128.95 BSC	
D3		2.175 BSC	
D4		6.62 BSC	
e1		64.77 BSC	
e2		49.53 BSC	
N		184	
E			4.10

Notes:

1 All dimensioning and tolerance conform to ASME Y14.5–1994.
2 Tolerance on all dimensions ± 0.13 unless otherwise specified.
3 All dimensions are in millimeters.
4 3.00mm minimum applies to both 4.00mm wide notch length and border of the component keepout area.
5 N is the total number of circuit contacts (Pins, Leads, TABS, or Pads.)