Datasheet | Rev. 3.0 | 2019

IMM512M72D2SRD8AG (Die Revision B) 4GByte (512M x 72 Bit)

4GB DDR2 Registered SO-DIMM
RoHS Compliant Product

Remark:
Please refer to the last page of the i) Contents ii) List of Table iii) List of Figures

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Features

- 200-Pin Registered Small Outline Dual-In-Line Memory Module
- Capacity: 4GB
- Maximum Data Transfer Rate: 6.40 GB/Sec
- JEDEC-Standard
- Power Supply: V_{DD}, V_{DDQ} = 1.8± 0.1 V
- Bi-directional Differential Data-Strobe (Single-ended data-strobe is an optional feature)
- 72 Bit Data Bus Width with ECC
- Programmable CAS Latency (CL):
  - PC2-6400: 4, 5, 6
  - PC2-5300: 4, 5
- Programmable Additive Latency (Posted /CAS): 0, CL-2 or CL-1(Clock)
- Write Latency (WL) = Read Latency (RC) - 1
- Posted /CAS
- On-Die Termination (ODT)
- Off-Chip Driver (OCD) Impedance Adjustment
- ZQ Calibration Supported
- Burst Type (Sequential & Interleave)
- Burst Length: 4, 8
- Refresh Mode: Auto and Self
- 8192 Refresh Cycles / 64ms
- Serial Presence Detect (SPD) with EEPROM
- SSTL_18 Interface
- Gold Edge Contacts
- 100% RoHS-Compliant
- Standard Module Height: 30.00mm (1.18 inch)

Table 1 - Ordering Information for RoHS Compliant Product

Part Number	Module Density	Configuration	# of Ranks	Module Type
IMM512M72D2SRD8AG-Bzzzy	4GB	512Mx72	2	4GB DDR2 Registered SO-DIMM

Notes:
y: Operating Temperature
zzz: Speed Grade

Table 2 - Temperature Grade

Part Number	Temperature Grade	T_{case}
Blank	Commercial temperature	0°C to 85°C
I	Industrial temperature	-40°C to 95°C

Remark: Tcase is the case surface temperature on the center/top side of the DRAM. The refresh rate is required to double when 85 °C < Tcase <= 95 °C.

Table 3 - Speed Grade

Part Number	Speed Grade	Max Clock Frequency (min. Clock Cycle time @ min. CAS Latency)
25	PC2-6400 (DDR2-800)	400MHz (2.5ns@CL=6)
3	PC2-5300 (DDR2-667)	333MHz (3.0ns@CL=5)

Table 4 - Memory Chip Information

Part Number	Base Device Brand	Base device	Voltage	Type	Chip Packing
IMM512M72D2SRD8AG-Bzzzy	I'M	IM2G08D2DBBG	1.8V	256Mx8	Lead Free

Part Number Decoder

IMM 512M72 D2 SR D 8 A G - B 25 (I)

Intelligent Memory Module

Module Configuration
512M72 = 512Mx72 (4GB)

Memory Type
D2 = DDR2

Module Form-Factor
SR = Registered SO-DIMM

Number of Ranks
D = Dual Ranks

DRAM Bit width
8 = using x8 components

Module PCB Revision
A = Revision A

RoHS compliance
G = Green / RoHS

IC Revision
B = Revision B

Speed Grade
3 = PC2-5300 / DDR2-667
25 = PC2-6400 / DDR2-800

Temperature Grade
Blank = Commercial Temperatu
(0°C to 85°C T_c)
I = Industrial Temperature
(-40°C to 95°C T_c)

Table 5 - Addressing

Parameter	4GB
Refresh count	8K
Row address	32K A[14:0]
Device bank address	8 BA[2:0]
Device configuration	2Gb (256Mx8)
Column address	1K A[9:0]
Module rank address	2 /S[1:0]
Number of devices	18

Table 6 - Pin Assignment

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{REF}	2	V_{SS}	101	V_{DD}	102	A6
3	D0	4	D4	103	A5	104	A4
5	V_{SS}	6	D5	105	A3	106	V_{DD}
7	D1	8	V_{SS}	107	A2	108	A1
9	/DQS0	10	DM0	109	V_{DD}	110	A0
11	DQS0	12	V_{SS}	111	A10, AP	112	BA1
13	V_{SS}	14	D6	113	BA0	114	V_{DD}
15	D2	16	D7	115	/RAS	116	/WE
17	D3	18	V_{SS}	117	V_{DD}	118	/S0
19	V_{SS}	20	D12	119	/CAS	120	ODT0
21	D8	22	D13	121	/S1	122	A13
23	D9	24	V_{SS}	123	V_{DD}	124	V_{DD}
25	V_{SS}	26	DM1	125	ODT1	126	CK
27	/DQS1	28	V_{SS}	127	NC	128	/CK
29	DQS1	30	D14	129	D32	130	V_{SS}
31	V_{SS}	32	D15	131	V_{SS}	132	D36
33	D10	34	V_{SS}	133	D33	134	D37
35	D11	36	D20	135	/DQS4	136	V_{SS}
37	V_{SS}	38	D21	137	DQS4	138	DM4
39	D16	40	V_{SS}	139	V_{SS}	140	V_{SS}
41	D17	42	/RESET	141	D34	142	D38
43	V_{SS}	44	DM2	143	D35	144	D39
45	/DQS2	46	V_{SS}	145	V_{SS}	146	V_{SS}
47	DQS2	48	D22	147	D40	148	D44
49	V_{SS}	50	D23	149	D41	150	D45
51	D18	52	V_{SS}	151	V_{SS}	152	V_{SS}
53	D19	54	D28	153	/DQS5	154	DM5
55	V_{SS}	56	D29	155	DQS5	156	V_{SS}
57	D24	58	V_{SS}	157	V_{SS}	158	D46
59	D25	60	DM3	159	D42	160	D47
61	V_{SS}	62	V_{SS}	161	D43	162	V_{SS}
63	/DQS3	64	D30	163	V_{SS}	164	D52
65	DQS3	66	D31	165	D48	166	D53
67	V_{SS}	68	V_{SS}	167	D49	168	V_{SS}
69	D26	70	CB4	169	V_{SS}	170	DM6
71	D27	72	CB5	171	/DQS6	172	V_{SS}
73	V_{SS}	74	V_{SS}	173	DQS6	174	D54
75	CB0	76	DM8	175	V_{SS}	176	D55
77	CB1	78	V_{SS}	177	D50	178	V_{SS}
79	V_{SS}	80	CB6	179	D51	180	D60
81	/DQS8	82	CB7	181	V_{SS}	182	D61
83	DQS8	84	V_{SS}	183	D56	184	V_{SS}
85	V_{SS}	86	CB2	185	D57	186	DM7
87	CKE0	88	CB3	187	V_{SS}	188	D62
89	CKE1	90	V_{SS}	189	/DQS7	190	V_{SS}
91	NC	92	BA2	191	DQS7	192	D63
93	V_{DD}	94	A14	193	D58	194	SDA
95	A12	96	A11	195	V_{SS}	196	SCL
97	A9	98	V_{DD}	197	D59	198	SA1
99	A7	100	A8	199	V_{DDSPD}	200	SA0

Table 7 - Pin Description			
Pin Name	Description	Pin Name	Description
V_{DD}	SDRAM core power supply	V_{SS}	Power supply return (ground)
V_{REF}	SDRAM I/O reference supply	V_{DDSPD}	EEPROM positive power supply
/RAS	SDRAM row address strobe	/CAS	SDRAM column address strobe
A0-A14	SDRAM address bus	/WE	SDRAM write enable
CKE0-CKE1	SDRAM clock enable line	BA0-BA2	SDRAM bank select
/S0-/S1	DIMM Rank Select Line	ODT0-ODT1	On-die termination control line
DQS0-DQS8	SDRAM data strobes (positive line of differential pair)	/DQS0-/DQS8	SDRAM data strobes (negative line of differential pair)
CK	SDRAM clocks (positive line of differential pair)	/CK	SDRAM clocks (negative line of differential pair)
D0-D63	DIMM memory data bus	CB0-CB7	Data check bits input/output
DM0-DM8	SDRAM data mask/high data strobes	/RESET	Register and PLL control pin
SCL	EEPROM clock	SDA	EEPROM data line
SA0-SA1	EEPROM address input	NC	Spare Pins (no connect)

Module Dimension

Figure 1 – Module Dimension 200 Pin DDR2 SDRAM Registered SO-DIMM

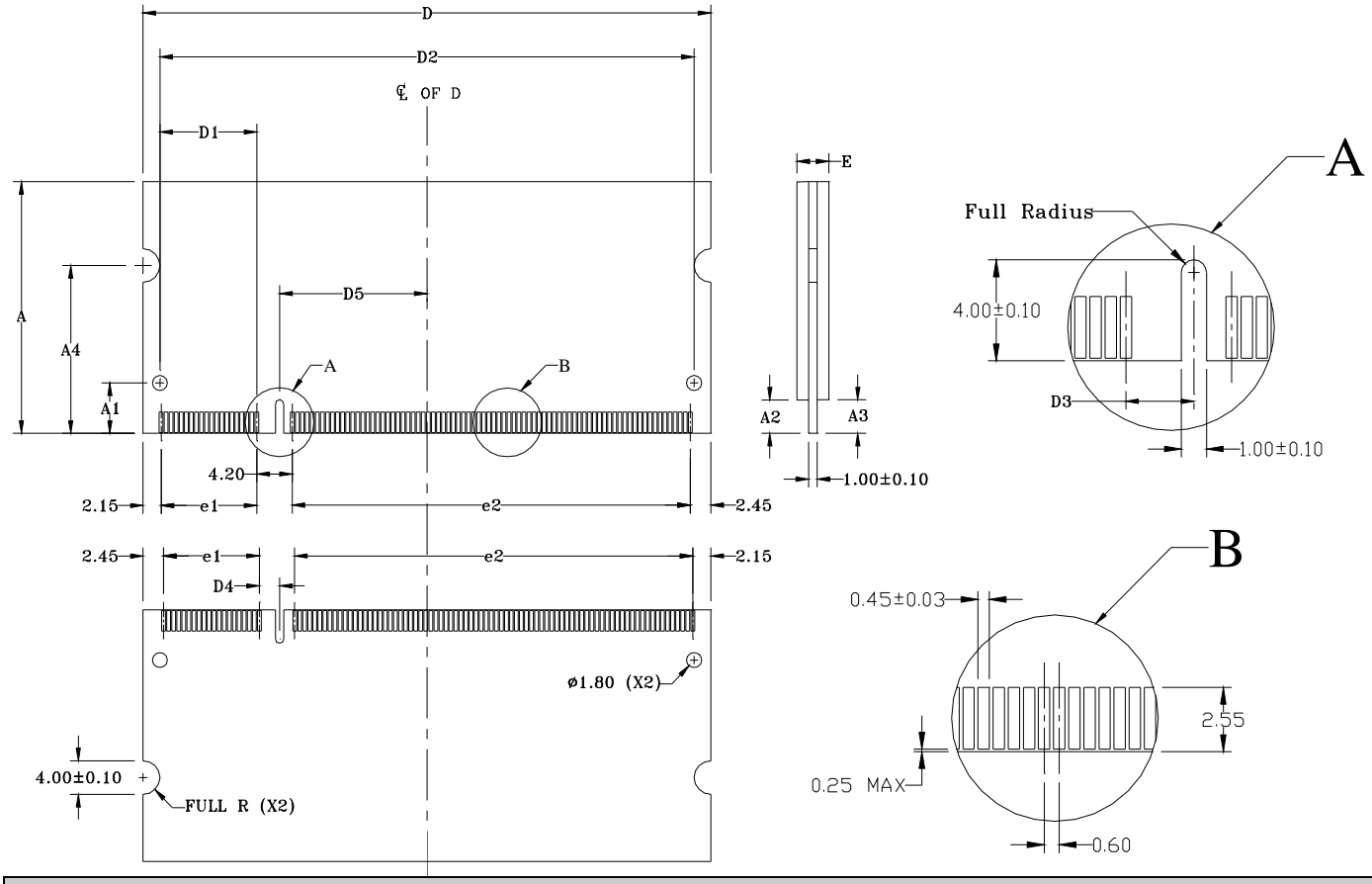


Table 8 - PCB Dimension

Symbol	MIN	NOM	MAX
A	29.85	30.00	30.15
A1		6.00 Basic	
A2	4.00		
A3	4.00		
A4		20.00 Basic	
D	67.45	67.60	67.75
D1		11.55 Basic	
D2		63.60 Basic	
D3		2.70 Basic	
D4		2.40 Basic	
D5		17.55 Basic	
e1		11.40 Basic	
e2		47.40 Basic	
E			3.80

Notes:

- All dimensioning and tolerancing conform to ASME Y14.5M-1994.
- Tolerances for all dimensions ±0.15 unless otherwise specified.
- All dimensions are in millimeters.

Figure 2 – Functional Block Diagram (Page 1 of 3)

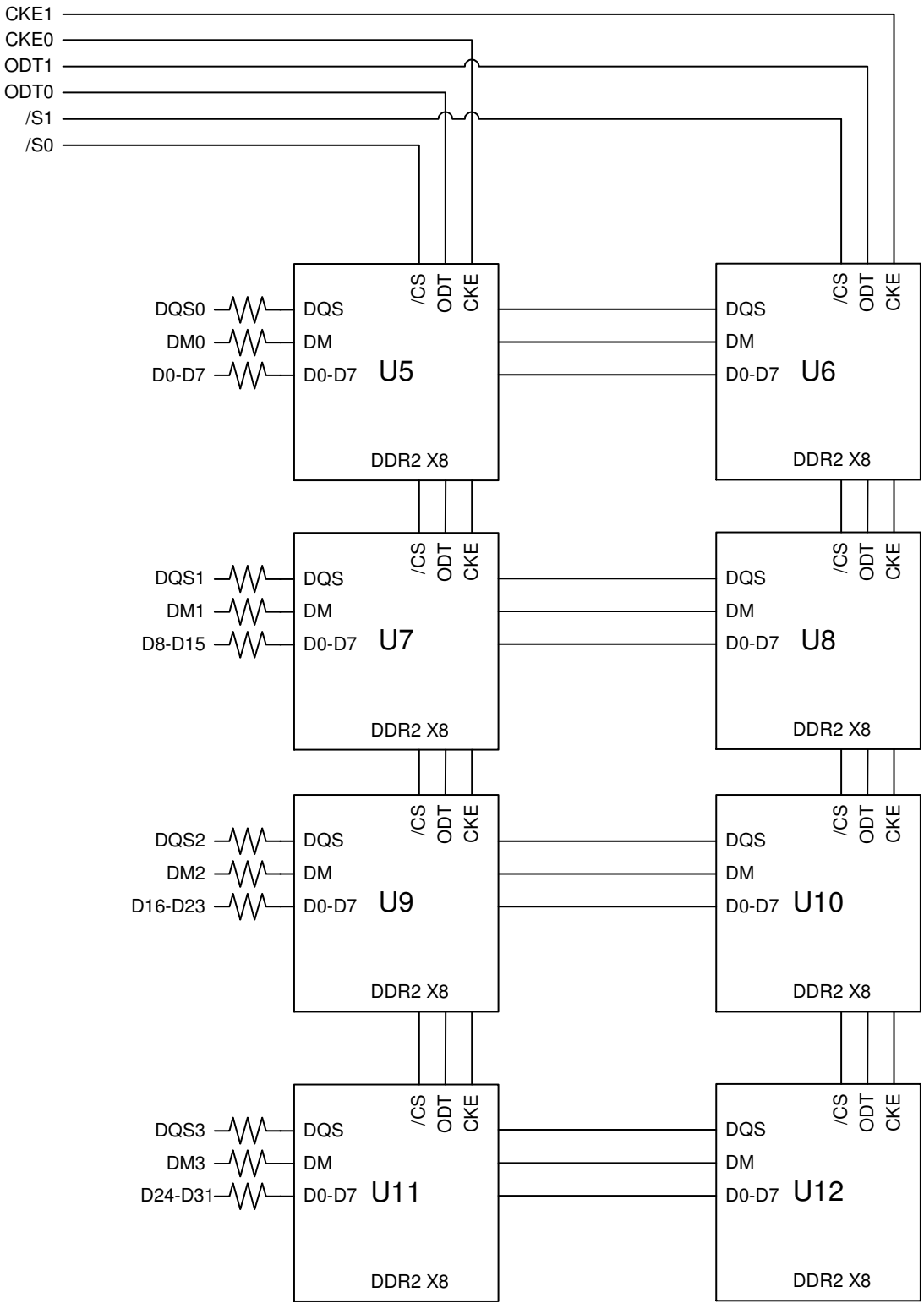


Figure 3 – Functional Block Diagram (Page 2 of 3)

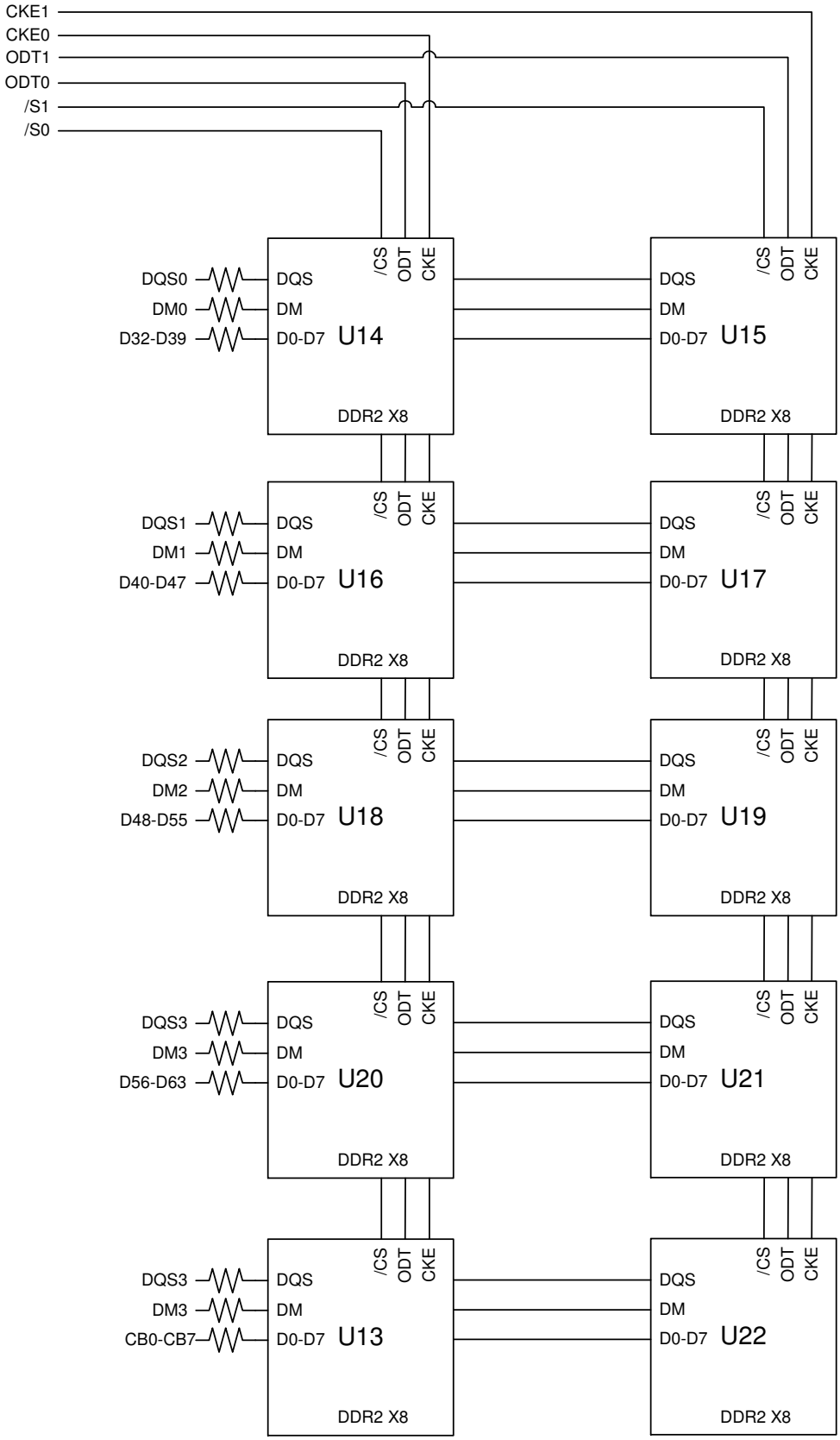
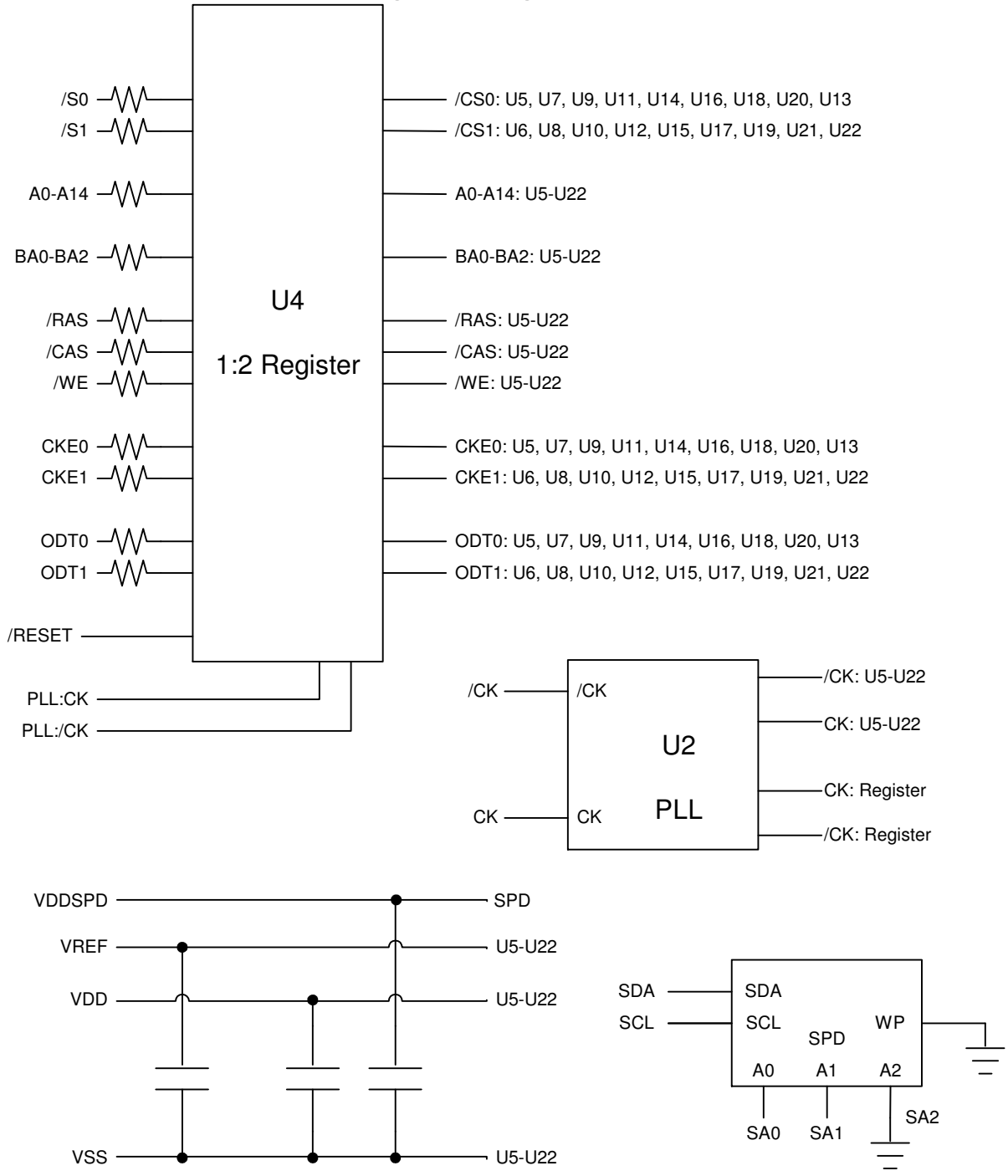


Figure 4 – Functional Block Diagram (Page 3 of 3)



Electrical Parameter

Table 9 – Absolute Maximum DC Ratings

Parameter	Symbol	Rating	Unit	Notes
Voltage on V_{DD} pin relative to V_{SS}	V_{DD}	-1.0V ~ 2.3V	V	1,3
Voltage on V_{DDQ} pin relative to V_{SS}	V_{DDQ}	-0.5V ~ 2.3V	V	1,3
Voltage on V_{DDL} pin relative to V_{SS}	V_{DDL}	-0.5V ~ 2.3V	V	1
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5V ~ 2.3V	V	1
DRAM Storage temperature	T_{STG}	-55 ~ +100	°C	1,2
DRAM Operation temperature (Standard Product)	T_{CASE}	0 ~ +85	°C	2,4
DRAM Operation temperature (Industrial Temperature Product)	T_{CASE}	-40 ~ +95	°C	2,5,6

Notes:

1 Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2 Storage Temperature or DRAM operation temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

3 V_{DD} and V_{DDQ} must be within 300mV of each other at all times; and V_{REF} must not be greater than 0.6 x V_{DDQ}, when V_{DD} and V_{DDQ} are less than 500mV; V_{REF} may be equal to or less than 300mV.

4 The Normal Temperature Range specifies the temperatures when all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0-85 °C under all operating conditions.

5 The Normal Temperature Range specifies the temperatures when all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between -40-95 °C under all operating conditions.

6 Some applications require operation of the Extended Temperature Range between 85 °C and 95 °C case temperature. Full Specifications are guaranteed in this range but the following additional conditions apply a) Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9us. b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b).

Table 10 - DC Electrical Characteristics and Operating Conditions

Parameter / Condition	Symbol	Rating			Units	Notes
		Min	Typ.	Max		
Supply voltage	V_{DD}	1.7	1.8	1.9	V	1
Supply voltage for I/O	V_{DDQ}	1.7	1.8	1.9	V	1
Supply voltage for DLL	V_{DDL}	1.7	1.8	1.9	V	1
Input Reference Voltage	V_{REF}	0.49 x V_{DDQ}	0.50 x V_{DDQ}	0.51 x V_{DDQ}	V	2,3
Termination Voltage	V_{TT}	V_{REF} -0.04	V_{REF}	V_{REF} +0.04	V	4

Notes:

1 V_{DDQ} tracks with V_{DD}, V_{DDL} tracks with V_{DD}. AC parameters are measured with V_{DD}, V_{DDQ} and V_{DDL} tied together.

2 The value of V_{REF} may be selected by the user to provide optimum noise margin in the system. Typically the value of V_{REF} is expected to be about 0.5 × V_{DDQ} of the transmitting device and V_{REF} is expected to track variations in V_{DDQ}.

3 Peak to peak ac noise on V_{REF} may not exceed ± 2% V_{REF} (dc)

4 V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in die dc level of V_{REF}

Table 11 - Input Switching Conditions

Parameter / Condition	Symbol	Value		Units
		Min	Max	
Input high AC voltage: Logic 1	$V_{IH(AC)}$	V_{REF} + 200	V_{DDQ} + V_{PEAK}	mV
Input high DC voltage: Logic 1	$V_{IH(DC)}$	V_{REF} + 125	V_{DDQ} + 300	mV
Input low AC voltage: Logic 0	$V_{IL(AC)}$	V_{SSQ} - V_{PEAK}	V_{REF} - 200	mV
Input low DC voltage: Logic 0	$V_{IL(DC)}$	-300	V_{REF} - 125	mV

Notes:

1. Single-ended input slew rate = 1 V/ns; maximum input voltage swing under test is 1.0V (peak-to-peak).

Table 12 - Differential Input and Output Operating Conditions (CK, /CK and DQS, /DQS)

Parameter / Condition	Symbol	Rating		Units	Notes
		Min	Max		
DC input signal voltage	$V_{IN(DC)}$	-300	V_{DDQ}+300	mV	1
DC differential input voltage	$V_{ID(DC)}$	250	V_{DDQ}+600	mV	2
AC differential input voltage	$V_{ID(AC)}$	500	V_{DDQ}	mV	3
AC differential cross point input voltage	$V_{IX(AC)}$	0.5 * V_{DDQ} - 175	0.5 * V_{DDQ} + 175	mV	4
AC differential cross point output voltage	$V_{OX(AC)}$	0.5 * V_{DDQ} - 125	0.5 * V_{DDQ} + 125	mV	5

Notes:

1. V_{IN}(dc) specifies the allowable DC execution of each input of differential pair.
2. V_{ID}(dc) specifies the input differential voltage V_{TR}– V_{CP} required for switching. The minimum value is equal to V_{IH}(dc) – V_{IL}(dc).
3. V_{ID}(ac) specifies the input differential voltage V_{TR} – V_{CP} required for switching. The minimum value is equal to V_{IH}(ac) – V_{IL}(ac).
4. The value of V_{IX}(ac) is expected to equal 0.5 × V_{DDQ} of the transmitting device and V_{IX}(ac) is expected to track variations in V_{DDQ}. V_{IX}(ac) indicates the voltage at which differential input signals must cross.
5. The value of V_{OX}(ac) is expected to equal 0.5 × V_{DDQ} of the transmitting device and V_{OX}(ac) is expected to track variations in V_{DDQ}. V_{OX}(ac) indicates the voltage at which differential input signals must cross.

For part number IMM512M72D2SRD8AG-B25(I)

Table 13 - IDD Specifications with Conditions and Operation Current

Parameter / Condition	Symbol	Current	Units	Notes
Operating current 0; One bank ACTIVATE-to-PRECHARGE	I_{DD0}	837	mA	1, 2
Operating current 1; One bank ACTIVATE-to-READ-to-PRECHARGE	I_{DD1}	963	mA	1, 2
Precharge power-down current	I_{DD2P}	216	mA	1, 3
Precharge standby current	I_{DD2N}	666	mA	1, 3
Precharge quiet standby current	I_{DD2Q}	648	mA	1, 3
Active power-down current (Fast Exit)	I_{DD3P0}	396	mA	1, 3
Active power-down current (Slow Exit)	I_{DD3P1}	396	mA	1, 3
Active standby current	I_{DD3N}	1044	mA	1, 3
Burst read operating current	I_{DD4R}	1503	mA	1, 2
Burst write operating current	I_{DD4W}	1521	mA	1, 2
Burst Auto-Refresh current	I_{DD5B}	1638	mA	1, 2
Distributed Auto-Refresh current	I_{DD5D}	495	mA	1, 2
Self-Refresh current	I_{DD6}	216	mA	1, 3
All banks interleaved read current	I_{DD7}	1998	mA	1, 2

Notes:
1 Value shown for DDR2 SDRAM only and are computed from values specified in the 2GBit component data sheet.
2 One module rank in the active IDD, the other rank in IDD2N.
3 All ranks in this IDD conditions.

For part number IMM512M72D2SRD8AG-B25(I)

Table 14 - AC Timing Parameter and Operating Conditions

Parameter / Condition		Symbol	Min	Max	Units
Clock Timing					
Clock period average: DLL disable mode	T_C = 0°C to 85°C	^tCK (DLL_DIS)	2.5	7.8	ns
	T_C => 85°C to 95°C		2.5	3.9	
Clock periods average: DLL enable mode (CL = 4, CWL = 3)		^tCK (AVG)	3.75	8.0	ns
Clock periods average: DLL enable mode (CL = 6, CWL = 4)		^tCK (AVG)	2.5	8.0	ns
High pulse width average		^tCH (AVG)	0.48	0.52	^tCK
Low pulse width average		^tCL (AVG)	0.48	0.52	^tCK
Clock period jitter	DLL locked	^tJITper	-100	100	ps
	DLL locking	$^tJITper,lck$	-80	80	ps
Clock absolute period		^tCK (ABS)	^tCK (AVG) MIN + ^tJITper MIN	^tCK (AVG) MAX + ^tJITper MAX	ps
Clock absolute high pulse width		^tCH (ABS)	^tCH (AVG) MIN x ^tCK (AVG) MIN + $^tJIT(DUTY)$ MIN	^tCH (AVG) MAX x ^tCK (AVG) MAX + $^tJIT(DUTY)$ MAX	ps
Clock absolute low pulse width		^tCL (ABS)	^tCL (AVG) MIN x ^tCK (AVG) MIN + $^tJIT(DUTY)$ MIN	^tCL (AVG) MAX x ^tCK (AVG) MAX + $^tJIT(DUTY)$ MAX	ps
Clock half pulse width		^tHP	Lower of ^tCH(ABS) or ^tCL(ABS)	-	ps
Cycle-to-cycle jitter	DLL locked	^tJITcc	-200	200	ps
	DLL locking	$^tJITcc,lck$	-160	160	ps
Duty-cycle jitter		$^tJIT(DUTY)$	-100	100	ps
Cumulative error across	2 cycles	$^tERR2per$	-150	150	ps
	3 cycles	$^tERR3per$	-175	175	ps
	4 cycles	$^tERR4per$	-200	200	ps
	5 cycles	$^tERR5per$	-200	200	ps
	6-10 cycles	$^tERR(6-10per)$	-300	300	ps
	11-50 cycles	$^tERR(11-50per)$	-450	450	ps
DQ Input Timing					
Data setup time to DQS, /DQS	Base (specification)	^tDS	50	-	ps
Data hold time from DQS, /DQS	Base (specification)	^tDH	125	-	ps
Minimum data pulse width		^tDIPW	0.35	-	^tCK
DQ Output Timing					
DQS, /DQS to DQ skew, per access		^tDQSQ	-	200	ps
DQ output access time from CK, /CK		^tAC	-400	400	ps
DQ output hold time from DQS, /DQS		^tQH	^tHP - ^tQHS	-	ps
DQ Hold skew factor		^tQHS	-	300	ps
DQ High-Z time from CK, /CK		^tHZ	-	$^tAC(MAX)$	ps
DQ Low-Z time from CK, /CK		^tLZDQ	2 x $^tAC(MIN)$	$^tAC(MAX)$	ps
DQ Strobe Input Timing					
DQS, /DQS rising to CK, /CK rising		^tDQSS	-0.25	0.25	^tCK
DQS, /DQS differential input low pulse width		^tDQSL	0.35	-	^tCK
DQS, /DQS falling setup to CK, /CK rising		^tDSS	0.2	-	^tCK
DQS, /DQS falling hold from CK, /CK rising		^tDSH	0.2	-	^tCK
DQS, /DQS differential input high pulse width		^tDQSH	0.35	-	^tCK

For part number IMM512M72D2SRD8AG-B25(I)

Parameter / Condition		Symbol	Min	Max	Units
DQS, /DQS differential WRITE preamble		tWPRE	0.35	-	tCK
DQS, /DQS differential WRITE postamble		tWPST	0.4	0.6	tCK
Write command to DQS associated clock edges		WL	RL - 1		tCK
DQ Strobe Output Timing					
DQS, /DQS rising to/from CK, /CK		tDQSCK	-350	350	ps
DQS, /DQS Low-Z time		tLZDQS	tAC(MIN)	tAC(MAX)	ps
DQS, /DQS differential READ preamble		tRPRE	0.9	1.1	tCK
DQS, /DQS differential READ postamble		tRPST	0.4	0.6	tCK
Command and Address Timing					
CTRL, CMD, ADDR setup to CK, /CK	Base (specification)	tIS	175	- -	ps
CTRL, CMD, ADDR hold from CK, /CK	Base (specification)	tIH	250	-	ps
Minimum CTRL, CMD, ADDR pulse width		tIPW	0.6	-	tCK
ACTIVATE to internal READ or WRITE delay		tRCD	12.5	-	ns
PRECHARGE command period		tRP	12.5	-	ns
ACTIVATE-to-PRECHARGE command period		tRAS	45	70k	ns
ACTIVATE-to-ACTIVATE command period		tRC	57.5	-	ns
ACTIVATE-to-ACTIVATE minimum period		tRRD	7.5	-	ns
Four ACTIVATE windows (1KB page size)		tFAW	35	-	ns
Write recovery time		tWR	15	-	ns
Delay from start of internal WRITE transaction to internal READ command		tWTR	7.5	-	ns
READ-to-PRECHARGE time		tRTP	7.5	-	ns
/CAS-to-/CAS command delay		tCCD	2	-	tCK
Auto precharge write recovery + precharge time		tDAL	WR + tRP/tCK (AVG)	-	tCK
MODE REGISTER SET command cycle time		tMRD	2	-	tCK
MODE REGISTER SET command update delay		tMOD	0	12	tCK
OCD drive mode output delay		tOIT	0	12	ns
Refresh Timing					
Auto Refresh Row Cycle Time		tRFC	195	-	ns
Maximum refresh period	T_c<=85°C	-	64 (1X)		ms
	T_c>85°C		32 (2X)		
Maximum average periodic refresh	T_c<=85°C	tREFI	-	7.8 (64ms/8192)	us
	T_c>85°C		-	3.9 (32ms/8192)	
Self Refresh Timing					
Exit self-refresh to a non-read command		tXSNR	tRFC+10	-	ns
Exit self refresh to read command		tXSRD	200	-	tCK
Minimum time clocks remain ON after CKE asynchronously drop LOW		tDELAY	tIS + tCKE (AVG) + tIH	-	tCK
Power-Down Timing					
CKE MIN pulse width		tCKE (MIN)	3	-	tCK
Power-Down Exit Timing					
Exist precharge power-down to any command		tXP	2	-	tCK
Exit active power down to read command		tXARD	2	-	tCK
Exit active power down to read command (slow exit, lower power)		tXARDS	8 - AL	-	tCK
ODT Timing					
R_{TT} turn-on from ODTL on reference		tAON	tAC(MIN)	tAC(MAX) + 0.7	ns
R_{TT} turn-off from ODTL off reference		tAOF	tAC(MIN)	tAC(MAX) + 0.6	tCK
ODT turn-on delay		tAOND	2	2	tCK

For part number IMM512M72D2SRD8AG-B25(I)

Parameter / Condition	Symbol	Min	Max	Units
ODT turn-off delay	^{t}AOFD	2.5	2.5	^{t}CK
Asynchronous R_{TT} turn-on delay (power-down with DLL off)	^{t}AONPD	^{t}AC(MIN) + 2	3 ^{t}CK + ^{t}AC(MAX) + 1	ns
Asynchronous R_{TT} turn-off delay (power-down with DLL off)	^{t}AOFPD	^{t}AC(MIN) + 2	2.5 ^{t}CK + ^{t}AC(MAX) + 1	ns
ODT to Power Down Mode Entry Latency	^{t}ANPD	3	-	^{t}CK
ODT to Power Down Mode Exit Latency	^{t}AXPD	8	-	^{t}CK

For part number IMM512M72D2SRD8AG-B25(I)

Table 15 - SPD Information

Byte NO.	Description	Note	Hex
0	Number of Serial PD Bytes written during module production	128	80
1	Total number of Bytes in Serial PD device	256 bytes	08
2	Fundamental Memory Type (FPM, EDO, SDRAM, DDR, DDR2…)	DDR2 SDRAM	08
3	Number of Row Addresses on this assembly	15	0F
4	Number of Column Addresses on this assembly	10	0A
5	Number of DIMM Ranks	30.00mm planar 2ranks	61
6	Data Width of this assembly	72bit	48
7	Reserved	Reserved	00
8	Voltage Interface Level of this assembly	SSTL _18	05
9	SDRAM Cycle time at Maximum Supported CAS Latency (CL), CL=X	2.5ns	25
10	SDRAM Access from Clock	0.4ns	40
11	DIMM configuration type (Non-parity, Parity or ECC)	ECC without Address / Command Parity	02
12	Refresh Rate/Type	7.8us	82
13	Primary SDRAM Width	x8	08
14	Error Checking SDRAM Width	x8	08
15	Reserved	Reserved	00
16	SDRAM Device Attributes: Burst Lengths Supported	4, 8	0C
17	SDRAM Device Attributes: Number of Banks on SDRAM Device	8 Banks	08
18	SDRAM Device Attributes: CAS Latency	4, 5, 6	70
19	DIMM Mechanical Characteristics	Undefined	00
20	DIMM Type Information	Registered SO-DIMM	07
21	SDRAM Module Attributes	1 PLL, 1 Registors	04
22	SDRAM Device Attributes: General	Supports 50 Ohm ODTTs, weak driver	03
23	Minimum Clock Cycle at CLX-1	3.0ns	30
24	Maximum Data Access Time (tAC) from Clock at CLX-1	0.45ns	45
25	Minimum Clock Cycle at CLX-2	3.75ns	3D
26	Maximum Data Access Time (tAC) from Clock at CLX-2	0.5ns	50
27	Minimum Row Precharge Time (tRP)	9.5ns	3C
28	Minimum Row Active to Row Active delay (tRRD)	7.5ns	1E
29	Minimum RAS to CAS delay (tRCD)	12.75ns	3C
30	Minimum Active to Precharge Time (tRAS)	45ns	2D
31	Module Rank Density	2GB	02
32	Address and Command Input Setup Time Before Clock (tIS)	0.17ns	17
33	Address and Command Input Hold Time After Clock (tIH)	0.25ns	25
34	Data Input Setup Time Before Strobe (tDS)	0.05ns	05
35	Data Input Hold Time After Strobe (tDH)	0.12ns	12
36	Write Recovery Time	12.75ns	3C
37	Internal write to read command delay (tWTR)	7.5ns	1E
38	Internal read to precharge command delay (tRTP)	7.5ns	1E
39	Memory Analysis Probe Characteristics	Reserved	00
40	Extension of Byte 41 tRC and Byte 42 tRFC	-	00

Byte NO.	Description	Note	Hex
41	SDRAM Device Minimum Active to Active/Refresh Time (tRC)	60ns	3C
42	SDRAM Device Minimum Refresh to Active/Refresh Command Period (tRFC)	195ns	C3
43	SDRAM Device Maximum device cycle time (tCKmax)	8.0ns	80
44	SDRAM Device maximum skew between DQS and DQ signals (tDQSQ)	0.20ns	14
45	SDRAM Device Maximum Read Data Hold Skew Factor (tQHS)	0.30ns	1E
46	PLL Relock Time	15us	0F
47	Bits 7:4: Tcasemax, Bits 3:0: DT4R4W Delta	Tcasemax = 85°C Not support DT4R4W Delta	00
48	Thermal resistance of DRAM device package from top (case) to ambient (Psi T-A DRAM)	Not supported	00
49	DRAM Case Temperature Rise from Ambient due to Activate-Precharge/Mode Bits (DT0/Mode Bits)	Not defined	00
50	DRAM Case Temperature Rise from Ambient due to Precharge/Quiet Standby (DT2N/DT2Q)	Not supported	00
51	DRAM Case Temperature Rise from Ambient due to Precharge Power-Down(DT2P)	Not supported	00
52	DRAM Case Temperature Rise from Ambient due to Active Standby (DT3N)	Not supported	00
53	DRAM Case temperature Rise from Ambient due to Active Power-Down with Fast PDN Exit (DT3Pfast)	Not supported	00
54	DRAM Case temperature Rise from Ambient due to Active Power-Down with Slow PDN Exit (DT3Pslow)	Not supported	00
55	DRAM Case Temperature Rise from Ambient due to Page Open Burst Read/ DT4R4W Mode Bit (DT4R/DT4R4W Mode Bit)	Not supported	00
56	DRAM Case Temperature Rise from Ambient due to Burst Refresh (DT5B)	Not supported	00
57	DRAM Case Temperature Rise from Ambient due to Bank Interleave Reads with Auto-Precharge (DT7)	Not supported	00
58	Thermal Resistance of PLL Package from Top (Case) to Ambient (Psi T-A PLL)	Not supported	00
59	Thermal Resistance of Register Package from Top (Case) to Ambient (Psi T-A Register)	Not supported	00
60	PLL Case Temperature Rise from Ambient due to PLL Active (DT PLL Active)	Not supported	00
61	Register Case Temperature Rise from Ambient due to Register Active/Mode Bit (DT Register Active/Mode Bit)	Not supported	00
62	SPD Revision	1.3	13
63	Checksum for Bytes 0-62	-	47
64-71	Manufacturer's JEDEC ID Code	Reserved	Reserved
72	Module Manufacturing Location	Reserved	Reserved
73-90	Module Part Number	Reserved	Reserved
91-92	Module Revision Code	Reserved	Reserved
93-94	Module Manufacturing Date	Reserved	Reserved
95-98	Module Serial Number	Reserved	Reserved
99-127	Manufacturer's Specific Data	Reserved	Reserved
128-255	Open for customer use	Reserved	Reserved

Revision History

Revision	Descriptions	Release Date
1.0	Initial released	Dec, 2013
2.0	Revised SPD information in table 16	Jan, 2015
3.0	Updated Memory Chip information in table 4	Dec, 2019

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