Datasheet | Rev. 1.0 | 2013

IMM512M72D2MRD8AG (Die Revision A)
4GByte (512M x 72 Bit)

4GB DDR2 Registered Mini-DIMM
RoHS Compliant Product

Version: Rev. 1.0, DEC 2013

1.0 - Initial release

Remark:
Please refer to the last page of the i) Contents ii) List of Table iii) List of Figures .

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Features

- 244-Pin Registered Mini Dual-In-Line Memory Module with Address and Command Parity
- Capacity: 4GB
- JEDEC-Standard
- Power Supply: VDD, VDDQ = 1.8± 0.1 V
- Bi-directional Differential Data-Strobe (Single-ended data-strobe is an optional feature)
- 72 Bit Data Bus Width with ECC
- Programmable CAS Latency (CL):
    - PC2-6400: 4, 5, 6
    - PC2-5300: 4, 5
- Programmable Additive Latency (Posted /CAS): 0, CL-2 or CL-1(Clock)
- Write Latency (WL) = Read Latency (RC) - 1
- Posted /CAS
- On-Die Termination (ODT)
- Off-Chip Driver (OCD) Impedance Adjustment
- ZQ Calibration Supported
- Burst Type (Sequential & Interleave)
- Burst Length: 4, 8
- Refresh Mode: Auto and Self
- 8192 Refresh Cycles / 64ms
- Serial Presence Detect (SPD) with EEPROM
- Gold Edge Contacts
- 100% RoHS-Compliant
- Standard Module Height: 30.00mm (1.181 inch)

Table 1 - Ordering Information for RoHS Compliant Product				
Part Number	Module Density	Configuration	# of Ranks	Module Type
IMM512M72D2MRD8AG-Azzzy	4GB	512Mx72	2	4GB DDR2 Registered Mini-DIMM

Notes:
y: Operating Temperature
zzz: Speed Grade

Table 2 - Temperature Grade		
Part Number	Temperature Grade	T_{case}
Blank	Commercial temperature	0°C to 85°C
I	Industrial temperature	-40°C to 95°C

Remark: Tcase is the case surface temperature on the center/top side of the DRAM. The refresh rate is required to double when 85 °C < Tcase <= 95 °C.

Table 3 - Speed Grade		
Part Number	Speed Grade	Max Clock Frequency (min. Clock Cycle time @ min. CAS Latency)
25	PC2-6400 (DDR2-800)	400MHz (2.5ns@CL=6)
3	PC2-5300 (DDR2-667)	333MHz (3.0ns@CL=5)

Table 4 - Memory Chip Information					
Part Number	Base Device Brand	Base device	Voltage	Type	Chip Packing
IMM512M72D2MRD8AG-Azzzy	Intelligent Memory	IM2G08D2DABG	1.8V	256Mx8	Lead Free

Part Number Decoder

IMM 512M72 D2 MR D 8 A G - A 25 I

Intelligent

Memory

Module

Module Configuration

512M72 = 512Mx72 (4GB)

Memory Type

D2 = DDR2

Module Form-Factor

MR = Registered Mini-DIMM

Number of Ranks

D = Dual Rank

Temperature Grade

Blank = Commercial Temperature

(0°C to 85°C T_C)

I = Industrial Temperature

(-40 to 95°C T_C)

Speed Grade

3 = PC2-5300 / DDR2-667

25 = PC2-6400 / DDR2-800

IC Revision

A = Revision A

B = Revision B

C = Revision C

RoHS-compliance

G = Green / RoHS

Module PCB Revision

A = Revision A

B = Revision B

C = Revision C

DRAM Bit width

8 = using x8 components

Table 5 - Addressing

Parameter	4GB
Refresh count	8K
Row address	64K A[14:0]
Device bank address	8 BA[2:0]
Device configuration	2Gb (256Mx8)
Column address	1K A[9:0]
Module rank address	2 /S[1:0]
Number of devices	18

Table 6 - Pin Assignment

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VREF	123	VSS	62	A4	184	VDDQ
2	VSS	124	DQ4	63	VDDQ	185	A3
3	DQ0	125	DQ5	64	A2	186	A1
4	DQ1	126	VSS	65	VDD	187	VDD
5	VSS	127	DM0	66	VSS	188	CK0
6	/DQS0	128	NC	67	VSS	189	/CK0
7	DQS0	129	VSS	68	NC	190	VDD
8	VSS	130	DQ6	69	VDD	191	A0
9	DQ2	131	DQ7	70	A10/AP	192	BA1
10	DQ3	132	VSS	71	BA0	193	VDD
11	VSS	133	DQ12	72	VDD	194	/RAS
12	DQ8	134	DQ13	73	/WE	195	VDDQ
13	DQ9	135	VSS	74	VDDQ	196	/S0
14	VSS	136	DM1	75	/CAS	197	VDDQ
15	/DQS1	137	NC	76	VDDQ	198	ODT0
16	DQS1	138	VSS	77	/S1	199	A13
17	VSS	139	RFU	78	ODT1	200	VDD
18	/RESET	140	RFU	79	VDDQ	201	NC
19	NC	141	VSS	80	NC	202	VSS
20	VSS	142	DQ14	81	VSS	203	DQ36
21	DQ10	143	DQ15	82	DQ32	204	DQ37
22	DQ11	144	VSS	83	DQ33	205	VSS
23	VSS	145	DQ20	84	VSS	206	DM4
24	DQ16	146	DQ21	85	/DQS4	207	NC
25	DQ17	147	VSS	86	DQS4	208	VSS
26	VSS	148	DM2	87	VSS	209	DQ38
27	/DQS2	149	NC	88	DQ34	210	DQ39
28	DQS2	150	VSS	89	DQ35	211	VSS
29	VSS	151	DQ22	90	VSS	212	DQ44
30	DQ18	152	DQ23	91	DQ40	213	DQ45
31	DQ19	153	VSS	92	DQ41	214	VSS
32	VSS	154	DQ28	93	VSS	215	DM5
33	DQ24	155	DQ29	94	/DQS5	216	NC
34	DQ25	156	VSS	95	DQS5	217	VSS
35	VSS	157	DM3	96	VSS	218	DQ46
36	/DQS3	158	NC	97	DQ42	219	DQ47
37	DQS3	159	VSS	98	DQ43	220	VSS
38	VSS	160	DQ30	99	VSS	221	DQ52
39	DQ26	161	DQ31	100	DQ48	222	DQ53
40	DQ27	162	VSS	101	DQ49	223	VSS
41	VSS	163	CB4	102	VSS	224	RFU
42	CB0	164	CB5	103	SA2	225	RFU
43	CB1	165	VSS	104	NC	226	VSS
44	VSS	166	DM8	105	VSS	227	DM6
45	/DQS8	167	NC	106	/DQS6	228	NC
46	DQS8	168	VSS	107	DQS6	229	VSS
47	VSS	169	CB6	108	VSS	230	DQ54
48	CB2	170	CB7	109	DQ50	231	DQ55
49	CB3	171	VSS	110	DQ51	232	VSS
50	VSS	172	NC	111	VSS	233	DQ60
51	NC	173	VDDQ	112	DQ56	234	DQ61
52	VDDQ	174	CKE1	113	DQ57	235	VSS
53	CKE0	175	VDD	114	VSS	236	DM7
54	VDD	176	NC	115	/DQS7	237	NC
55	BA2	177	A14	116	DQS7	238	VSS
56	NC	178	VDDQ	117	VSS	239	DQ62
57	VDDQ	179	A12	118	DQ58	240	DQ63
58	A11	180	A9	119	DQ59	241	VSS
59	A7	181	VDD	120	VSS	242	SDA

Pin	Name	Pin	Name	Pin	Name	Pin	Name
60	VDD	182	A8	121	SA0	243	SCL
61	A5	183	A6	122	SA1	244	VDDSPD

Table 7 - Pin Description

Pin Name	Description	Pin Name	Description
VDD	SDRAM core power supply	VREFDQ	SDRAM I/O reference supply
VREFCA	SDRAM command/address reference supply	VSS	Power supply return (ground)
A0-A14	SDRAM address bus	BA0-BA2	SDRAM bank addresses
CK0-CK1	SDRAM clocks (positive line of differential pair)	/CK0-/CK1	SDRAM clocks (negative line of differential pair)
/RAS	SDRAM row address strobe	/CAS	SDRAM column address strobe
/WE	SDRAM write enable	CKE0-CKE1	SDRAM clock enable lines
/S0-/S1	DIMM Rank Select Lines	ODT0-ODT1	On-die termination control lines
DQS0-DQS8	SDRAM data strobes (positive line of differential pair)	/DQS0-/DQS8	SDRAM data strobes (negative line of differential pair)
D0-D63	DIMM memory data bus	DM0-DM8	SDRAM data mask/high data strobes
CB0-CB7	Data check bits Input/Output	SDA	EEPROM date line
SCL	EEPROM clock	VDDSPD	EEPROM positive power supply
SA0-SA1	EEPROM address input	/RESET	Reset Pin
NC	Spare Pins (no connect)		

Figure 1 – Module Dimension 244 Pin DDR2 SDRAM Registered Mini-DIMM

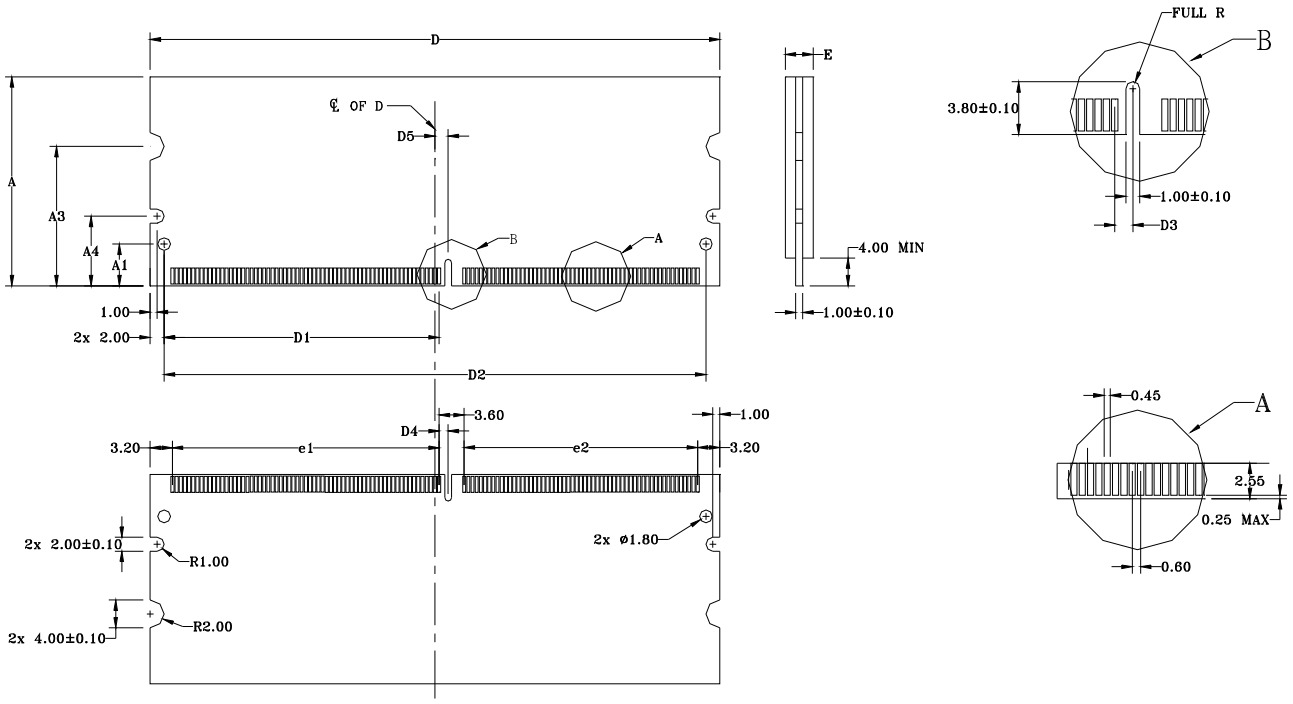


Table 8 - PCB Dimension			
Symbol	MIN	NOM	MAX
A	29.85	30.00	30.15
A1		6.00 Basic	
A3		20.00 Basic	
A4		10.00 Basic	
D	81.85	82.00	82.15
D1		39.60 Basic	
D2		78.00 Basic	
D3		1.30 Basic	
D4		1.30 Basic	
D5		1.90 Basic	
e1		38.40 Basic	
e2		33.60 Basic	
E			3.80

Notes:

- All dimensioning and tolerancing conform to ASME Y14.5M-1994.
- Tolerances for all dimensions ±0.15 unless otherwise specified.
- All dimensions are in millimeters.

Figure 2 – Functional Block Diagram (Page 1 of 3)

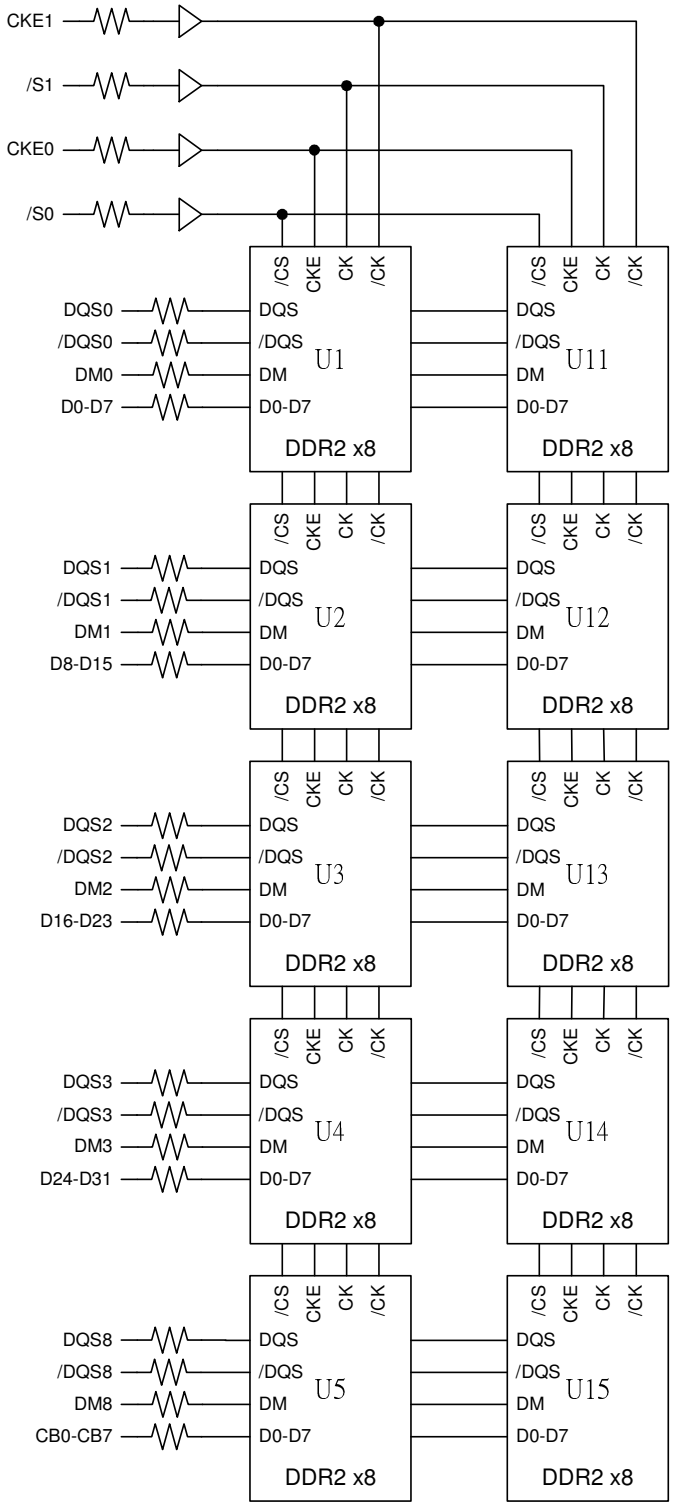


Figure 3 – Functional Block Diagram (Page 2 of 3)

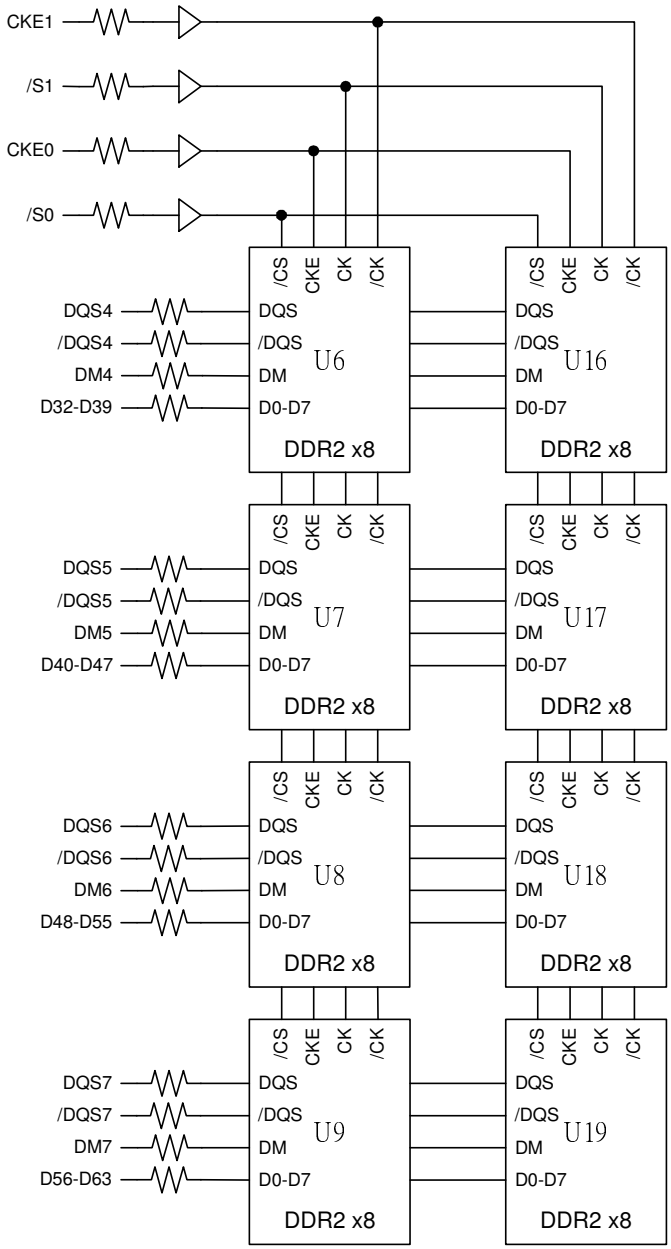
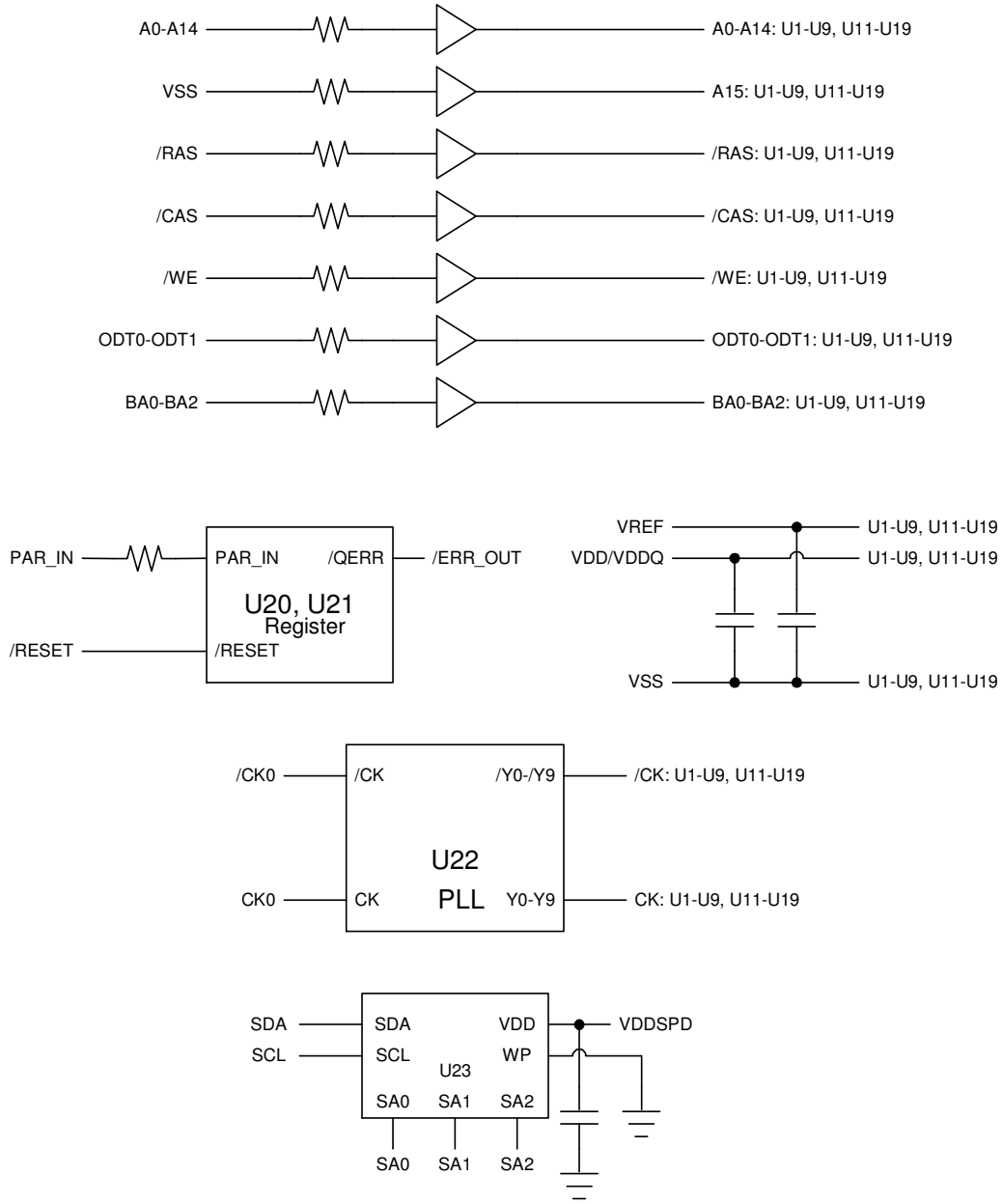


Figure 4 – Functional Block Diagram (Page 3 of 3)



Electrical Parameter

Table 9 - Absolute Maximum DC Ratings

Parameter	Symbol	Rating	Unit	Notes
Voltage on V_{DD} pin relative to V_{SS}	V_{DD}	-1.0V ~ 2.3	V	1,3
Voltage on V_{DDQ} pin relative to V_{SS}	V_{DDQ}	-0.5V ~ 2.3	V	1,3
Voltage on V_{DDL} pin relative to V_{SS}	V_{DDL}	-0.5V ~ 2.3	V	1
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5V ~ 2.3	V	1
DRAM Storage temperature	T_{STG}	-55 ~ 100	°C	1,2
DRAM Operation temperature (Standard Product)	T_{CASE}	0 ~ 85	°C	2,4
DRAM Operation temperature (Industrial Temperature Product)	T_{CASE}	-40 ~ 95	°C	2,5,6

Notes:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature or DRAM operation temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300mV of each other at all times; and VREF must not be greater than 0.6 x VDDQ, when VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.
4. The Normal Temperature Range specifies the temperatures when all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0-85 °C under all operating conditions.
5. The Normal Temperature Range specifies the temperatures when all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between -40-95 °C under all operating conditions.
6. Some applications require operation of the Extended Temperature Range between 85 °C and 95 °C case temperature. Full Specifications are guaranteed in this range but the following additional conditions apply a) Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9us. b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b).

Table 10 - DC Electrical Characteristics and Operating Conditions

Parameter / Condition	Symbol	Rating			Units	Notes
		Min	Typ.	Max		
Supply voltage	V_{DD}	1.7	1.8	1.9	V	1
Supply voltage for I/O	V_{DDQ}	1.7	1.8	1.9	V	1
Supply voltage for DLL	V_{DDL}	1.7	1.8	1.9	V	1
Input Reference Voltage	V_{REF}	0.49 x V_{DDQ}	1.5 x V_{DDQ}	0.51 x V_{DDQ}	V	2,3
Termination Voltage	V_{TT}	V_{REF} -0.04	V_{REF}	V_{REF} +0.04	V	4

Notes:

1 VDDQ tracks with VDD, VDDL tracks with VDD. AC parameters are measured with VDD, VDDQ and VDDL tied together.

2 The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about 0.5 × VDDQ of the transmitting device and VREF is expected to track variations in VDDQ.

3 Peak to peak ac noise on VREF may not exceed ± 2% VREF (dc)

4 VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF, and must track variations in die dc level of VREF

Table 11 - Input and Output Leakage Currents

Symbol	Parameter / Condition	Value		Unit	Note
		Min.	Max.		
I_{IL}	Input Leakage Current; any input 0V < V_{IN} < V_{DD}	-2	+2	µA	1
I_{OL}	Output Leakage Current; 0V < V_{OUT} < V_{DDQ}	-5	+5	µA	2

Note

1 All other pins not under test = 0 V

2 DQ's, LDQS, /LDQS, UDQS, /UDQS, DQS, /DQS, RDQS, /RDQS are disabled and ODT is turned off

Table 12 - Input Switching Conditions

Parameter / Condition	Symbol	Value		Units
		Min	Max	
Input high AC voltage: Logic 1	$V_{IH(AC)}$	V_{REF} + 200	V_{DDQ} + V_{PEAK}	mV
Input high DC voltage: Logic 1	$V_{IH(DC)}$	V_{REF} + 125	V_{DDQ} + 300	mV
Input low DC voltage: Logic 0	$V_{IL(DC)}$	-300	V_{REF} - 125	mV
Input low AC voltage: Logic 0	$V_{IL(AC)}$	V_{SSQ} - V_{PEAK}	V_{REF} - 200	mV

Notes:

1. Single-ended input slew rate = 1 V/ns; maximum input voltage swing under test is 1.0V (peak-to-peak).

Table 13 - Differential Input and Output Operating Conditions (CK, /CK and DQS, /DQS)					
Parameter / Condition	Symbol	Rating		Units	Notes
		Min	Max		
DC input signal voltage	$V_{IN(DC)}$	-300	V_{DDQ} + 300	mV	1
DC differential input voltage	$V_{ID(DC)}$	250	V_{DDQ} + 600	mV	2
AC differential input voltage	$V_{ID(AC)}$	500	V_{DDQ} + 600	mV	3
AC differential cross point input voltage	$V_{IX(AC)}$	0.5 * V_{DDQ} - 175	0.5 * V_{DDQ} + 175	mV	4
AC differential cross point output voltage	$V_{OX(AC)}$	0.5 * V_{DDQ} - 125	0.5 * V_{DDQ} + 125	mV	5

Notes:

1. V_{IN}(dc) specifies the allowable DC execution of each input of differential pair.
2. V_{ID}(dc) specifies the input differential voltage V_{TR}– V_{CP} required for switching. The minimum value is equal to V_{IH}(dc) – V_{IL}(dc).
3. V_{ID}(ac) specifies the input differential voltage V_{TR} – V_{CP} required for switching. The minimum value is equal to V_{IH}(ac) – V_{IL}(ac).
4. The value of V_{IX}(ac) is expected to equal 0.5 × V_{DDQ} of the transmitting device and V_{IX}(ac) is expected to track variations in V_{DDQ}. V_{IX}(ac) indicates the voltage at which differential input signals must cross.
5. The value of V_{OX}(ac) is expected to equal 0.5 × V_{DDQ} of the transmitting device and V_{OX}(ac) is expected to track variations in V_{DDQ}. V_{OX}(ac) indicates the voltage at which differential input signals must cross.

For part number IMM512M72D2MRD8AG-A25(I)

Table 14 - IDD Specifications with Conditions and Operation Current

Parameter / Condition	Symbol	Current	Units	Notes
Operating current 0; One bank ACTIVATE-to-PRECHARGE	I_{DD0}	756	mA	1, 2
Operating current 1; One bank ACTIVATE-to-READ-to-PRECHARGE	I_{DD1}	828	mA	1, 2
Precharge power-down current	I_{DD2P}	216	mA	1, 3
Precharge standby current	I_{DD2N}	900	mA	1, 3
Precharge quiet standby current	I_{DD2Q}	810	mA	1, 3
Active power-down current (Fast Exit)	I_{DD3P0}	288	mA	1, 3
Active power-down current (Slow Exit)	I_{DD3P1}	288	mA	1, 3
Active standby current	I_{DD3N}	990	mA	1, 3
Burst read operating current	I_{DD4R}	1323	mA	1, 2
Burst write operating current	I_{DD4W}	1188	mA	1, 2
Refresh current	I_{DD5B}	1548	mA	1, 2
Distributed Refresh current	I_{DD5D}	252	mA	1, 2
Self refresh temperature current: MAX T_c = 85°C	I_{DD6}	216	mA	1, 3
Self refresh temperature current (SRT-enabled): MAX T_c = 95°C	I_{DD6ET}	324	mA	1, 3
All banks interleaved read current	I_{DD7}	1908	mA	1, 2

Notes:

1. Value shown for DDR2 SDRAM only and are computed from values specified in the 2GBit component data sheet.
2. One module rank in the active IDD, the other rank in IDD2P.
3. All ranks in this IDD conditions.

For part number IMM512M72D2MRD8AG-A25(I)

Table 15 - AC Timing Parameter and Operating Conditions

Parameter / Condition		Symbol	Min	Max	Units
Clock Timing					
Clock period average: DLL disable mode	T_C = 0°C to 85°C	^tCK (DLL_DIS)	2.5	7.8	ns
	T_C => 85°C to 95°C		2.5	3.9	
Clock periods average: DLL enable mode (CL = 4, CWL = 3)		^tCK (AVG)	3.0	<3.75	ns
Clock periods average: DLL enable mode (CL = 6, CWL = 4)		^tCK (AVG)	2.5	<3.0	ns
High pulse width average		^tCH (AVG)	0.48	0.52	^tCK
Low pulse width average		^tCL (AVG)	0.48	0.52	^tCK
Clock period jitter	DLL locked	^tJITper	-100	100	ps
	DLL locking	$^tJITper,lck$	-80	80	ps
Clock absolute period		^tCK (ABS)	^tCK (AVG) MIN + ^tJITper MIN	^tCK (AVG) MAX + ^tJITper MAX	ps
Clock absolute high pulse width		^tCH (ABS)	^tCH (AVG) MIN x ^tCK (AVG) MIN + $^tJIT(DUTY)$ MIN	^tCH (AVG) MAX x ^tCK (AVG) MAX + $^tJIT(DUTY)$ MAX	ps
Clock absolute low pulse width		^tCL (ABS)	^tCL (AVG) MIN x ^tCK (AVG) MIN + $^tJIT(DUTY)$ MIN	^tCL (AVG) MAX x ^tCK (AVG) MAX + $^tJIT(DUTY)$ MAX	ps
Clock half pulse width		^tHP	Lower of ^tCH(ABS) or ^tCL(ABS)	-	ps
Cycle-to-cycle jitter	DLL locked	^tJITcc	-200	200	ps
	DLL locking	$^tJITcc,lck$	-160	160	ps
Duty-cycle jitter		$^tJIT(DUTY)$	-100	100	ps
Cumulative error across	2 cycles	$^tERR2per$	-150	150	ps
	3 cycles	$^tERR3per$	-175	175	ps
	4 cycles	$^tERR4per$	-200	200	ps
	5 cycles	$^tERR5per$	-200	200	ps
	6-10 cycles	$^tERR(6-10per)$	-300	300	ps
	11-50 cycles	$^tERR(11-50per)$	-450	450	ps
DQ Input Timing					
Data setup time to DQS, /DQS	Base (specification)	^tDS	50	-	ps
					ps
Data hold time from DQS, /DQS	Base (specification)	^tDH	125	-	ps
					ps
Minimum data pulse width		^tDIPW	0.35	-	^tCK
DQ Output Timing					
DQS, /DQS to DQ skew, per access		^tDQSQ	-	200	ps
DQ output access time from CK, /CK		^tAC	-400	400	ps
DQ output hold time from DQS, /DQS		^tQH	^tHP - ^tQHS	-	ps
DQ Hold skew factor		^tQHS	-	300	ps
DQ High-Z time from CK, /CK		^tHZ	-	$^tAC(MAX)$	ps
DQ Low-Z time from CK, /CK		^tLZDQ	2 x $^tAC(MIN)$	$^tAC(MAX)$	ps
DQ Strobe Input Timing					
DQS, /DQS rising to CK, /CK rising		^tDQSS	-0.25	0.25	^tCK
DQS, /DQS differential input low pulse width		^tDQSL	0.35	-	^tCK

For part number IMM512M72D2MRD8AG-A25(I)

Parameter / Condition		Symbol	Min	Max	Units
DQS, /DQS falling setup to CK, /CK rising		tDSS	0.2	-	tCK
DQS, /DQS falling hold from CK, /CK rising		tDSH	0.2	-	tCK
DQS, /DQS differential input high pulse width		tDQSH	0.35	-	tCK
DQS, /DQS differential WRITE preamble		tWPRE	0.35	-	tCK
DQS, /DQS differential WRITE postamble		tWPST	0.4	0.6	tCK
Write command to DQS associated clock edges		WL	RL - 1		tCK
DQ Strobe Output Timing					
DQS, /DQS rising to/from CK, /CK		tDQSCK	-350	350	ps
DQS, /DQS Low-Z time		tLZDQS	tAC(MIN)	tAC(MAX)	ps
DQS, /DQS differential READ preamble		tRPRE	0.9	1.1	tCK
DQS, /DQS differential READ postamble		tRPST	0.4	0.6	tCK
Command and Address Timing					
CTRL, CMD, ADDR setup to CK, /CK	Base (specification)	tIS	175	- -	ps
CTRL, CMD, ADDR hold from CK, /CK	Base (specification)	tIH	250	-	ps
Minimum CTRL, CMD, ADDR pulse width		tIPW	0.6	-	tCK
ACTIVATE to internal READ or WRITE delay		tRCD	12.5	-	ns
PRECHARGE command period		tRP	12.5	-	ns
ACTIVATE-to-PRECHARGE command period		tRAS	45	70k	ns
ACTIVATE-to-ACTIVATE command period		tRC	57.5	-	ns
ACTIVATE-to-ACTIVATE minimum period		tRRD	7.5	-	ns
Four ACTIVATE windows (1KB page size)		tFAW	35	-	ns
Write recovery time		tWR	15	-	ns
Internal WRITE-to-READ delay		tWTR	7.5	-	ns
READ-to-PRECHARGE time		tRTP	7.5	-	ns
/CAS-to-/CAS command delay		tCCD	2	-	tCK
Auto precharge write recovery + precharge time		tDAL	WR + tRP/tCK (AVG)	-	tCK
MODE REGISTER SET command cycle time		tMRD	2	-	tCK
MODE REGISTER SET command update delay		tMOD	0	12	tCK
OCD drive mode output delay		tOIT	0	12	ns

For part number IMM512M72D2MRD8AG-A25(I)

Parameter / Condition		Symbol	Min	Max	Units
Refresh Timing					
REFRESH-to-ACTIVATE or REFRESH command period		tRFC	195	-	ns
Maximum refresh period	T_c<=85°C	-	64 (1X)		ms
	T_c>85°C		32 (2X)		
Maximum average periodic refresh	T_c<=85°C	tREFI	-	7.8 (64ms/8192)	us
	T_c>85°C		-	3.9 (32ms/8192)	
Self Refresh Timing					
Exit self refresh to non-read command		tXSNR	tRFC+10	-	ns
Exit self refresh to read command		tXSRD	200	-	ns
Minimum time clocks remain ON after CKE asynchronously drops LOW		tDELAY	tIS + tCKE (AVG) + tIH	-	ns
Power-Down Timing					
CKE MIN pulse width		tCKE (MIN)	3	-	tCK
Power-Down Exit Timing					
Exit precharge pown-down to any command		tXP	2	-	tCK
Exit active power down to read command		tXARD	2	-	tCK
Exit active power down to read command (slow exit, lower power)		tXARDS	8 - AL	-	tCK
ODT Timing					
R_{TT} turn-on from ODTL on reference		tAON	tAC(MIN)	tAC(MAX) + 0.7	ns
R_{TT} turn-off from ODTL off reference		tAOF	tAC(MIN)	tAC(MAX) + 0.6	ns
ODT turn-on delay		tAOND	2	2	tCK
ODT turn-off delay		tAOFD	2.5	2.5	tCK
Asynchronous R_{TT} turn-on delay (power-down with DLL off)		tAONPD	tAC(MIN) + 2	2 tCK + tAC(MAX) + 1	ns
Asynchronous R_{TT} turn-off delay (power-down with DLL off)		tAOFPD	tAC(MIN) + 2	2.5 tCK + tAC(MAX) + 1	ns
ODT to Power Down Mode Entry Latency		tANPD	3	-	tCK
ODT to Power Down Mode Exit Latency		tAXPD	8	-	tCK

For part number IMM512M72D2MRD8AG-A25(I)

Table 16 - SPD Information

Byte NO.	Description	Note	Hex
0	Number of Serial PD Bytes written during module production	128	80
1	Total number of Bytes in Serial PD device	256 bytes	08
2	Fundamental Memory Type (FPM, EDO, SDRAM, DDR, DDR2…)	DDR2 SDRAM	08
3	Number of Row Addresses on this assembly	15	0F
4	Number of Column Addresses on this assembly	10	0A
5	Number of DIMM Ranks	30.0mm planar 2ranks	61
6	Data Width of this assembly	72bit	48
7	Reserved	Reserved	00
8	Voltage Interface Level of this assembly	SSTL _18	05
9	SDRAM Cycle time at Maximum Supported CAS Latency (CL), CL=X	2.5ns	25
10	SDRAM Access from Clock	0.4ns	40
11	DIMM configuration type (Non-parity, Parity or ECC)	ECC with Address / Command Parity	06
12	Refresh Rate/Type	7.8us	82
13	Primary SDRAM Width	x8	08
14	Error Checking SDRAM Width	x8	08
15	Reserved	Reserved	00
16	SDRAM Device Attributes: Burst Lengths Supported	4, 8	0C
17	SDRAM Device Attributes: Number of Banks on SDRAM Device	8 Banks	08
18	SDRAM Device Attributes: CAS Latency	4, 5, 6	70
19	DIMM Mechanical Characteristics	Undefined	00
20	DIMM Type Information	Registered Mini-DIMM	10
21	SDRAM Module Attributes	1 PLL, 2 Registors	05
22	SDRAM Device Attributes: General	Supports 50 Ohm ODTTs, weak driver	03
23	Minimum Clock Cycle at CLX-1	3.0ns	30
24	Maximum Data Access Time (tAC) from Clock at CLX-1	0.45ns	45
25	Minimum Clock Cycle at CLX-2	3.75ns	3D
26	Maximum Data Access Time (tAC) from Clock at CLX-2	0.5ns	50
27	Minimum Row Precharge Time (tRP)	9.5ns	3C
28	Minimum Row Active to Row Active delay (tRRD)	7.5ns	1E
29	Minimum RAS to CAS delay (tRCD)	12.75ns	3C
30	Minimum Active to Precharge Time (tRAS)	45ns	2D
31	Module Rank Density	2GB	02
32	Address and Command Input Setup Time Before Clock (tIS)	0.17ns	17
33	Address and Command Input Hold Time After Clock (tIH)	0.25ns	25
34	Data Input Setup Time Before Strobe (tDS)	0.05ns	05
35	Data Input Hold Time After Strobe (tDH)	0.12ns	12
36	Write Recovery Time	12.75ns	3C
37	Internal write to read command delay (tWTR)	7.5ns	1E
38	Internal read to precharge command delay (tRTP)	7.5ns	1E
39	Memory Analysis Probe Characteristics	Reserved	00
40	Extension of Byte 41 tRC and Byte 42 tRFC	-	00
41	SDRAM Device Minimum Active to Active/Refresh Time (tRC)	60ns	3C

Byte NO.	Description	Note	Hex
42	SDRAM Device Minimum Refresh to Active/Refresh Command Period (tRFC)	195ns	C3
43	SDRAM Device Maximum device cycle time (tCKmax)	8.0ns	80
44	SDRAM Device maximum skew between DQS and DQ signals (tDQSQ)	0.20ns	14
45	SDRAM Device Maximum Read Data Hold Skew Factor (tQHS)	0.30ns	1E
46	PLL Relock Time	15us	0F
47	Bits 7:4: Tcasemax, Bits 3:0: DT4R4W Delta	Tcasemax = 85°C Not support DT4R4W Delta	00
48	Thermal resistance of DRAM device package from top (case) to ambient (Psi T-A DRAM)	Not supported	00
49	DRAM Case Temperature Rise from Ambient due to Activate-Precharge/Mode Bits (DT0/Mode Bits)	Not defined	00
50	DRAM Case Temperature Rise from Ambient due to Precharge/Quiet Standby (DT2N/DT2Q)	Not supported	00
51	DRAM Case Temperature Rise from Ambient due to Precharge Power-Down(DT2P)	Not supported	00
52	DRAM Case Temperature Rise from Ambient due to Active Standby (DT3N)	Not supported	00
53	DRAM Case temperature Rise from Ambient due to Active Power-Down with Fast PDN Exit (DT3Pfast)	Not supported	00
54	DRAM Case temperature Rise from Ambient due to Active Power-Down with Slow PDN Exit (DT3Pslow)	Not supported	00
55	DRAM Case Temperature Rise from Ambient due to Page Open Burst Read/ DT4R4W Mode Bit (DT4R/DT4R4W Mode Bit)	Not supported	00
56	DRAM Case Temperature Rise from Ambient due to Burst Refresh (DT5B)	Not supported	00
57	DRAM Case Temperature Rise from Ambient due to Bank Interleave Reads with Auto-Precharge (DT7)	Not supported	00
58	Thermal Resistance of PLL Package from Top (Case) to Ambient (Psi T-A PLL)	Not supported	00
59	Thermal Resistance of Register Package from Top (Case) to Ambient (Psi T-A Register)	Not supported	00
60	PLL Case Temperature Rise from Ambient due to PLL Active (DT PLL Active)	Not supported	00
61	Register Case Temperature Rise from Ambient due to Register Active/Mode Bit (DT Register Active/Mode Bit)	Not supported	00
62	SPD Revision	1.1	11
63	Checksum for Bytes 0-62	-	53
64-71	Manufacturer's JEDEC ID Code	Reserved	Reserved
72	Module Manufacturing Location	Reserved	Reserved
73-90	Module Part Number	Reserved	Reserved
91-92	Module Revision Code	Reserved	Reserved
93-94	Module Manufacturing Date	Reserved	Reserved
95-98	Module Serial Number	Reserved	Reserved
99-127	Manufacturer's Specific Data	Reserved	Reserved
128-255	Open for customer use	Reserved	Reserved

Contents

List of Tables

List of Figures