Datasheet | Rev. 1.0 | 2019

IMM1G72D2RDD4AG (Die Revision B)
8GByte (1024M x 72 Bit)

8GB DDR2 Registered DIMM
RoHS Compliant Product

Remark:
Please refer to the last page of the i) Contents ii) List of Table iii) List of Figures.

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Features

- 240-Pin Registered Dual-In-Line Memory Module with Address and Command Parity
- Capacity: 8GB
- JEDEC-Standard
- Power Supply: VDD, VDDQ = 1.8± 0.1V
- Bi-directional Differential Data-Strobe (Single-ended data-strobe is an optional feature)
- 72 Bit Data Bus Width with ECC
- Programmable CAS Latency (CL):
  - PC2-6400: 4, 5, 6
  - PC2-5300: 4, 5
- Programmable Additive Latency (Posted /CAS): 0, CL-2 or CL-1(Clock)
- Posted /CAS
- On-Die Termination (ODT)
- Off-Chip Driver (OCD) Impedance Adjustment
- Burst Type (Sequential & Interleave)
- Burst Length: 4, 8
- Refresh Mode: Auto and Self
- 8192 Refresh Cycles / 64ms
- Serial Presence Detect (SPD) with EEPROM
- SSTL-18 Interface
- Gold Edge Contacts
- 100% RoHS-Compliant
- Standard Module Height: 30.00 mm (1.181 inch)

Table 1 - Ordering Information for RoHS Compliant Product

Part Number	Module Density	Configuration	# of Ranks	Module Type
IMM1G72D2RDD4AG-Bzzzy	8GB	1Gx72	2	8GB DDR2 Registered DIMM

Notes:
y: Operating Temperature
zzz: Speed Grade

Table 2 - Temperature Grade

Part Number	Temperature Grade	T_{case}
Blank	Commercial temperature	0°C to 95°C
I	Industrial temperature	-40°C to 95°C

Remark: Tcase is the case surface temperature on the center/top side of the DRAM. The refresh rate is required to double when 85 °C < Tcase <= 95 °C.

Table 3 - Speed Grade

Part Number	Speed Grade	Max. Clock Frequency (min. Clock Cycle time @ min. CAS Latency)
25	PC2-6400 (DDR2-800)	400MHz (2.5ns@CL=6)
3	PC2-5300 (DDR2-667)	333MHz (3.0ns@CL=5)

Table 4 - Memory Chip Information

Part Number	Base Device Brand	Base device	Voltage	Type	Chip Packing
IMM1G72D2RDD4AG-Bzzzy	I'M	IM2G04D2DBBG	1.8V	512Mx4	Lead Free

Part Number Decoder

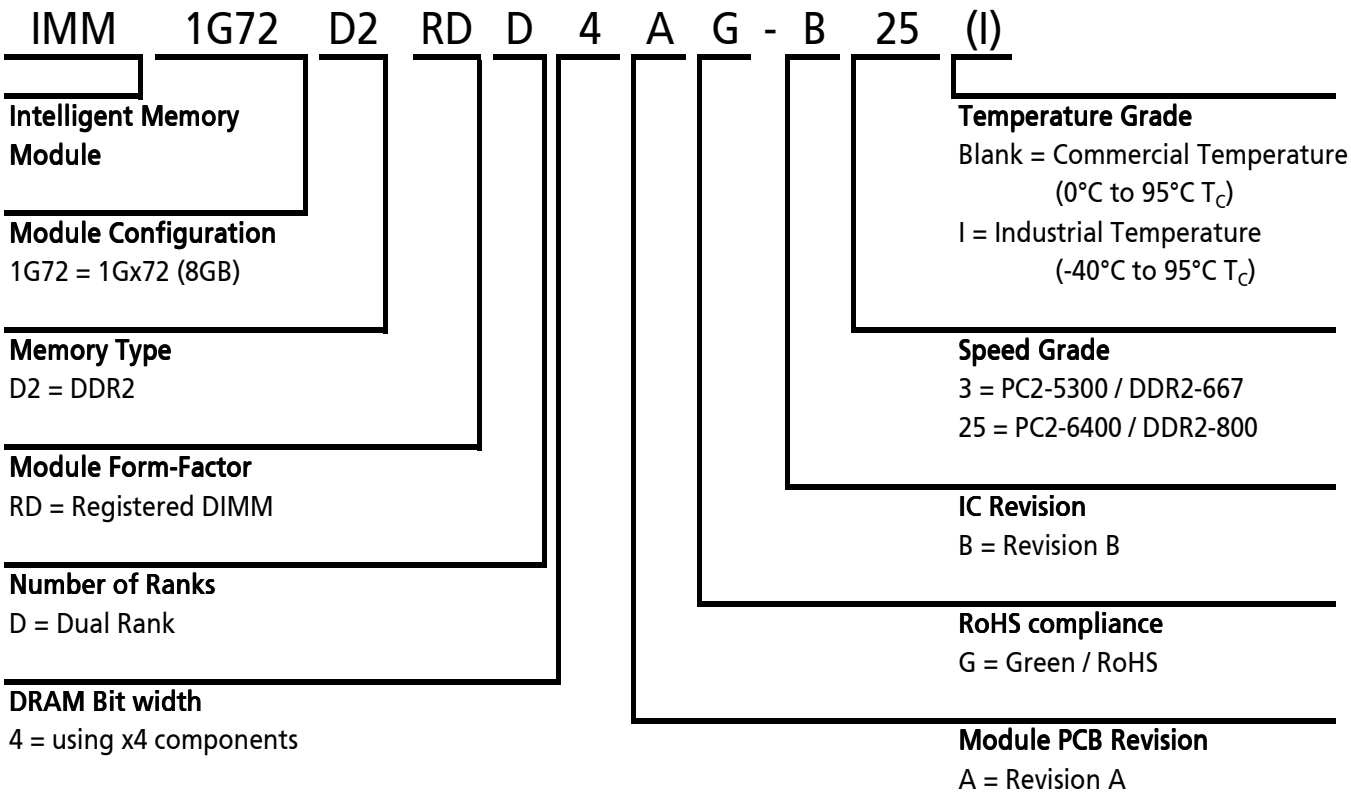


Table 5 - Addressing

Parameter	8GB
Refresh count	8K
Row address	32K A[14:0]
Device bank address	8 BA[2:0]
Device configuration	2Gb (512Mx4)
Column address	2K A[9:0], A11
Module rank address	2 /S[1:0]
Number of devices	36

Table 6 - Pin Assignment

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{REF}	121	V_{SS}	61	A4	181	V_{DDQ}
2	V_{SS}	122	D4	62	V_{DDQ}	182	A3
3	D0	123	D5	63	A2	183	A1
4	D1	124	V_{SS}	64	V_{DD}	184	V_{DD}
5	V_{SS}	125	DQS9	65	V_{SS}	185	CK0
6	/DQS0	126	/DQS9	66	V_{SS}	186	/CK0
7	DQS0	127	V_{SS}	67	V_{DD}	187	V_{DD}
8	V_{SS}	128	D6	68	Par_In	188	A0
9	D2	129	D7	69	V_{DD}	189	V_{DD}
10	D3	130	V_{SS}	70	A10 / AP	190	BA1
11	V_{SS}	131	D12	71	BA0	191	V_{DDQ}
12	D8	132	D13	72	V_{DDQ}	192	/RAS
13	D9	133	V_{SS}	73	/WE	193	/S0
14	V_{SS}	134	DQS10	74	/CAS	194	V_{DDQ}
15	/DQS1	135	/DQS10	75	V_{DDQ}	195	ODT0
16	DQS1	136	V_{SS}	76	/S1	196	A13
17	V_{SS}	137	CK1	77	ODT1	197	V_{DD}
18	NC	138	/CK1	78	V_{DDQ}	198	V_{SS}
19	NC	139	V_{SS}	79	V_{SS}	199	D36
20	V_{SS}	140	D14	80	D32	200	D37
21	D10	141	D15	81	D33	201	V_{SS}
22	D11	142	V_{SS}	82	V_{SS}	202	DQS13
23	V_{SS}	143	D20	83	/DQS4	203	/DQS13
24	D16	144	D21	84	DQS4	204	V_{SS}
25	D17	145	V_{SS}	85	V_{SS}	205	D38
26	V_{SS}	146	DQS11	86	D34	206	D39
27	/DQS2	147	/DQS11	87	D35	207	V_{SS}
28	DQS2	148	V_{SS}	88	V_{SS}	208	D44
29	V_{SS}	149	D22	89	D40	209	D45
30	D18	150	D23	90	D41	210	V_{SS}
31	D19	151	V_{SS}	91	V_{SS}	211	DQS14
32	V_{SS}	152	D28	92	/DQS5	212	/DQS14
33	D24	153	D29	93	DQS5	213	V_{SS}
34	D25	154	V_{SS}	94	V_{SS}	214	D46
35	V_{SS}	155	DQS12	95	D42	215	D47
36	/DQS3	156	/DQS12	96	D43	216	V_{SS}
37	DQS3	157	V_{SS}	97	V_{SS}	217	D52
38	V_{SS}	158	D30	98	D48	218	D53
39	D26	159	D31	99	D49	219	V_{SS}
40	D27	160	V_{SS}	100	V_{SS}	220	CK2
41	V_{SS}	161	CB4	101	SA2	221	/CK2
42	CB0	162	CB5	102	NC	222	V_{SS}
43	CB1	163	V_{SS}	103	V_{SS}	223	DQS15
44	V_{SS}	164	DQS17	104	/DQS6	224	/DQS15
45	/DQS8	165	/DQS17	105	DQS6	225	V_{SS}
46	DQS8	166	V_{SS}	106	V_{SS}	226	D54
47	V_{SS}	167	CB6	107	D50	227	D55
48	CB2	168	CB7	108	D51	228	V_{SS}
49	CB3	169	V_{SS}	109	V_{SS}	229	D60
50	V_{SS}	170	V_{DDQ}	110	D56	230	D61
51	V_{DDQ}	171	CKE1	111	D57	231	V_{SS}
52	CKE0	172	V_{DD}	112	V_{SS}	232	DQS16
53	V_{DD}	173	NC	113	/DQS7	233	/DQS16
54	BA2	174	A14	114	DQS7	234	V_{SS}
55	/Err_out	175	V_{DDQ}	115	V_{SS}	235	D62
56	V_{DDQ}	176	A12	116	D58	236	D63
57	A11	177	A9	117	D59	237	V_{SS}
58	A7	178	V_{DD}	118	V_{SS}	238	V_{DDSPD}
59	V_{DD}	179	A8	119	SDA	239	SA0
60	A5	180	A6	120	SCL	240	SA1

Table 7 - Pin Description

Pin Name	Description	Pin Name	Description
V_{DD}	SDRAM core power supply	V_{REF}	SDRAM I/O reference supply
A0-A14	SDRAM address bus	V_{SS}	Power supply return (ground)
CK0-CK1	SDRAM clocks (positive line of differential pair)	BA0-BA2	SDRAM bank addresses
/RAS	SDRAM row address strobe	/CK0-/CK1	SDRAM clocks (negative line of differential pair)
/WE	SDRAM write enable	/CAS	SDRAM column address strobe
/S0-/S1	DIMM Rank Select Lines	CKE0-CKE1	SDRAM clock enable lines
/RESET	Reset Pin	ODT0-ODT1	On-die termination control lines
DQS0-DQS17	SDRAM data strobes (positive line of differential pair)	/DQS0-/DQS17	SDRAM data strobes (negative line of differential pair)
D0-D63	DIMM memory data bus	CB0-CB7	Data check bits Input/Output
/Err_Out	Parity error found in the Address and Control bus	SDA	EEPROM date line
Par_In	Parity bit for the Address and Control bus	SCL	EEPROM clock
NC	Spare Pins (no connect)	SA0-SA1	EEPROM address input
V_{DDSPD}	EEPROM positive power supply	-	-

Module Dimension

Figure 1 – 240 Pin DDR2 SDRAM Registered DIMM

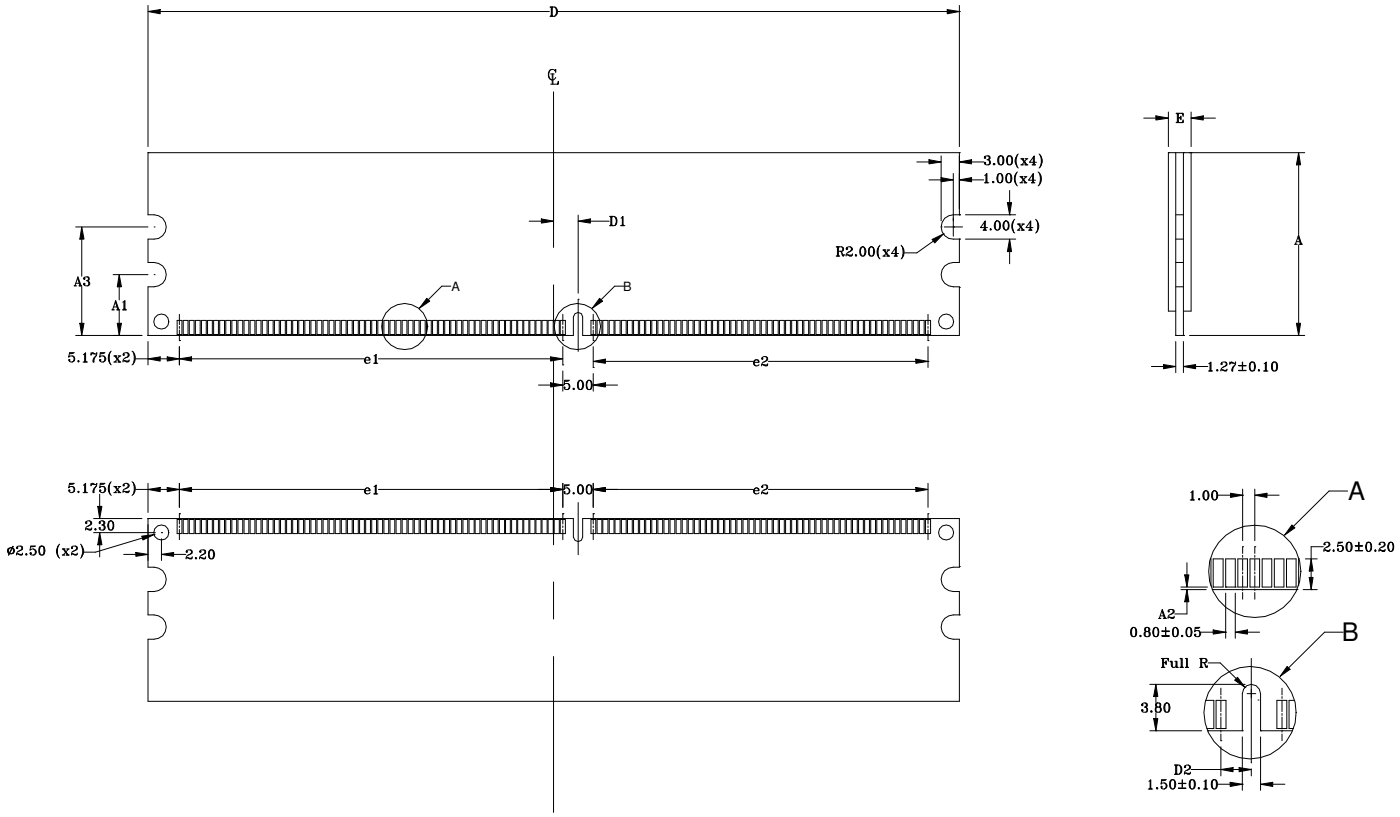


Table 8 - PCB Dimension			
Symbol	MIN	NOM	MAX
A	29.85	30.00	30.15
A1		10.00 Basic	
A2	0.05	0.20	0.35
A3		17.80 Basic	
D	133.20	133.35	133.50
D1		4.00 Basic	
D2		2.50 Basic	
e1		63.00 Basic	
e2		55.00 Basic	
E			4.00

Notes:

- All dimensioning and tolerancing conform to ASME Y14.5M-1994.
- Tolerances for all dimensions ±0.15 unless otherwise specified.
- All dimensions are in millimeters.

Figure 2 – Functional Block Diagram (Page 1 of 3)

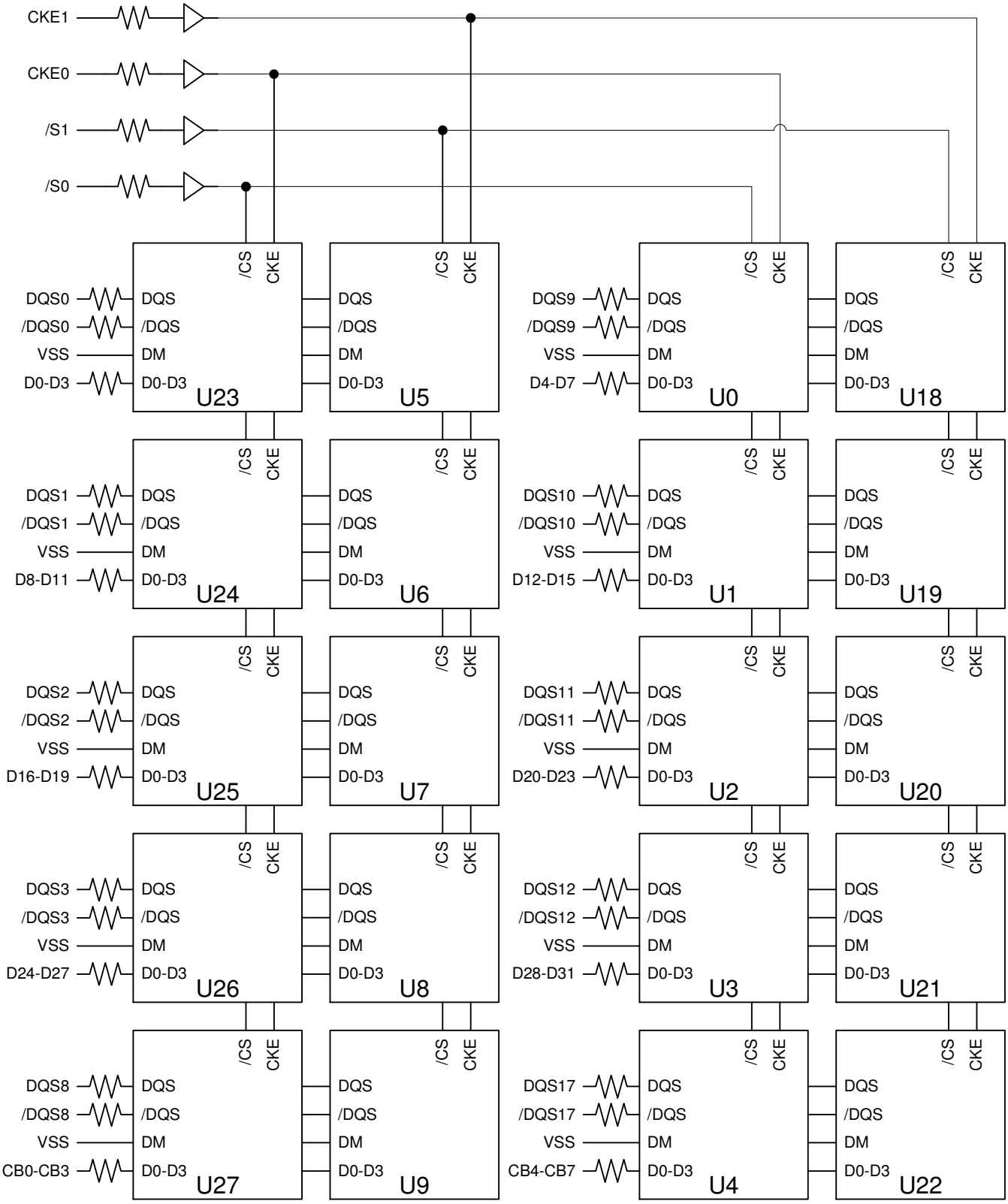


Figure 3 – Functional Block Diagram (Page 2 of 3)

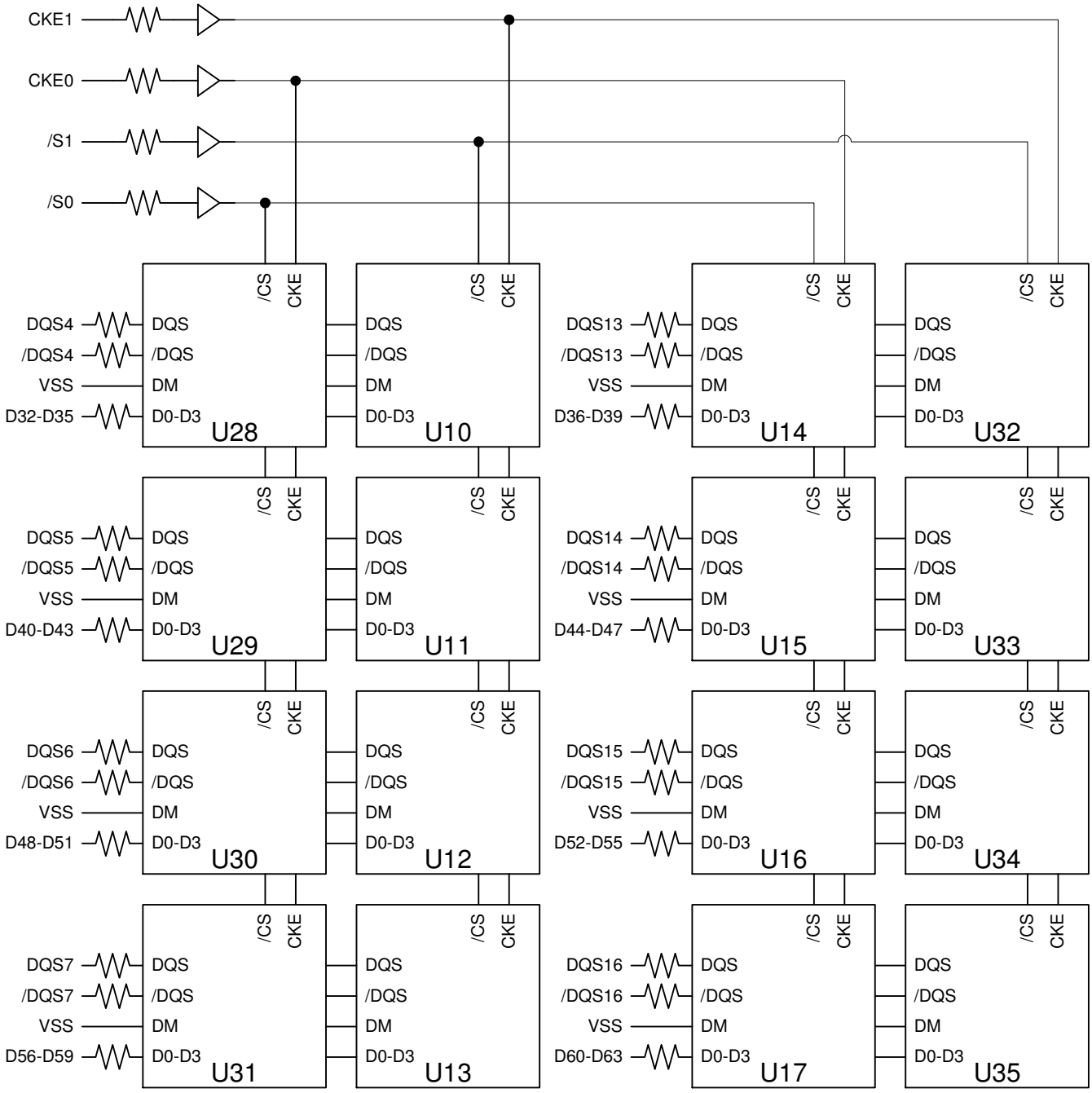
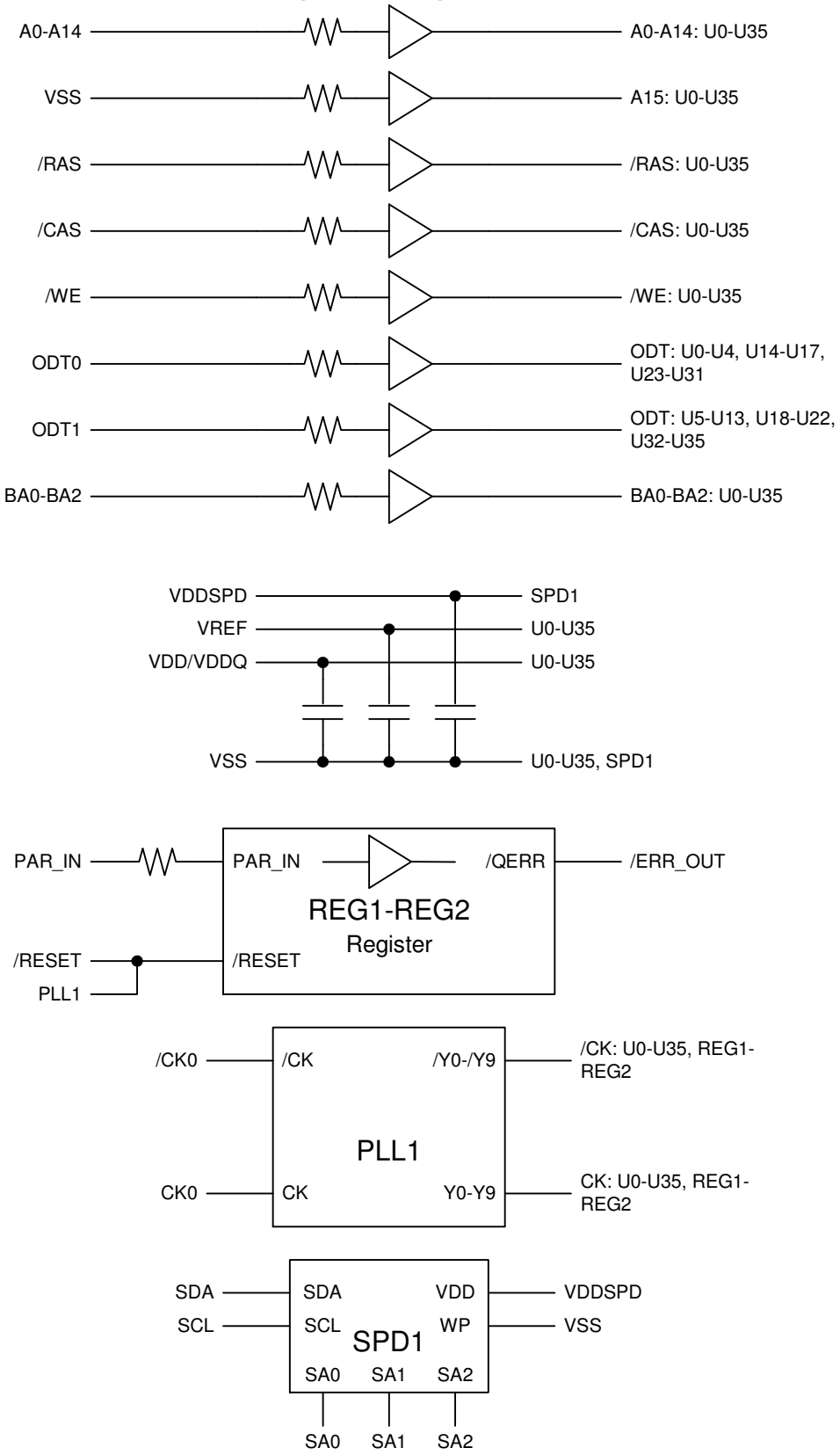


Figure 4 – Functional Block Diagram (Page 3 of 3)



Electrical Parameter

Table 9 – Absolute Maximum DC Ratings

Parameter	Symbol	Rating	Unit	Notes
Voltage on V_{DD} pin relative to V_{SS}	V_{DD}	-1.0V ~ 2.3	V	1,3
Voltage on V_{DDQ} pin relative to V_{SS}	V_{DDQ}	-0.5V ~ 2.3	V	1,3
Voltage on V_{DDL} pin relative to V_{SS}	V_{DDL}	-0.5V ~ 2.3	V	1
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5V ~ 2.3	V	1
DRAM Storage temperature	T_{STG}	-55 ~ 100	°C	1,2
DRAM Operation temperature (Standard Product)	T_{CASE}	0 ~ 85	°C	2,4,6
DRAM Operation temperature (Industrial Temperature Product)	T_{CASE}	-40 ~ 95	°C	2,5,6

Notes:

1 Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2 Storage Temperature or DRAM operation temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

3 VDD and VDDQ must be within 300mV of each other at all times; and VREF must not be greater than 0.6 x VDDQ, when VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.

4 The Normal Temperature Range specifies the temperatures when all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0-85 °C under all operating conditions.

5 The Normal Temperature Range specifies the temperatures when all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between -40-95 °C under all operating conditions.

6 Some applications require operation of the Extended Temperature Range between 85 °C and 95 °C case temperature. Full Specifications are guaranteed in this range but the following additional conditions apply a) Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9us. b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b).

Table 10 - DC Electrical Characteristics and Operating Conditions

Parameter / Condition	Symbol	Rating			Units	Notes
		Min	Typ	Max		
Supply voltage	V_{DD}	1.7	1.8	1.9	V	1
Supply voltage for I/O	V_{DDQ}	1.7	1.8	1.9	V	1
Supply voltage for DLL	V_{DDL}	1.7	1.8	1.9	V	1
Input Reference Voltage	V_{REF}	0.49 x V_{DDQ}	0.5 x V_{DDQ}	0.51 x V_{DDQ}	V	2,3
Termination Voltage	V_{TT}	V_{REF} -0.04	V_{REF}	V_{REF} +0.04	V	4

Notes:

1 VDDQ tracks with VDD, VDDL tracks with VDD. AC parameters are measured with VDD, VDDQ and VDDL tied together.

2 The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about 0.5 × VDDQ of the transmitting device and VREF is expected to track variations in VDDQ.

3 Peak to peak ac noise on VREF may not exceed ± 2% VREF (dc)

4 VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF, and must track variations in die dc level of VREF

Table 11 - Input Switching Conditions

Parameter / Condition	Symbol	Value		Units
		Min	Max	
Input high AC voltage: Logic 1	$V_{IH(AC)}$	V_{REF} + 200	V_{DDQ} + V_{PEAK}	mV
Input high DC voltage: Logic 1	$V_{IH(DC)}$	V_{REF} + 125	V_{DDQ} + 300	mV
Input low DC voltage: Logic 0	$V_{IL(DC)}$	-300	V_{REF} - 125	mV
Input low AC voltage: Logic 0	$V_{IL(AC)}$	V_{SSQ} - V_{PEAK}	V_{REF} - 200	mV

Notes:

1. Single-ended input slew rate = 1 V/ns; maximum input voltage swing under test is 1.0V (peak-to-peak).

Table 12 - Differential Input and Output Operating Conditions (CK, /CK and DQS, /DQS)

Parameter / Condition	Symbol	Rating		Units	Notes
		Min	Max		
AC differential input voltage	$V_{ID(AC)}$	500	V_{DDQ}	mV	1
AC differential cross point input voltage	$V_{IX(AC)}$	0.5 * V_{DDQ} - 175	0.5 * V_{DDQ} + 175	mV	2
AC differential cross point output voltage	$V_{OX(AC)}$	0.5 * V_{DDQ} - 125	0.5 * V_{DDQ} + 125	mV	3

Notes:

1. V_{ID}(ac) specifies the input differential voltage V_{TR} – V_{CP} required for switching. The minimum value is equal to V_{IH}(ac) – V_{IL}(ac).
2. The value of V_{IX}(ac) is expected to equal 0.5 × V_{DDQ} of the transmitting device and V_{IX}(ac) is expected to track variations in V_{DDQ}. V_{IX}(ac) indicates the voltage at which differential input signals must cross.
3. The value of V_{OX}(ac) is expected to equal 0.5 × V_{DDQ} of the transmitting device and V_{OX}(ac) is expected to track variations in V_{DDQ}. V_{OX}(ac) indicates the voltage at which differential input signals must cross.

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Table 13 - IDD Specifications with Conditions and Operation Current

Parameter / Condition	Symbol	Current	Units	Notes
Operating current 0; One bank ACTIVATE-to-PRECHARGE	I_{DD0}	1674	mA	1, 2
Operating current 1; One bank ACTIVATE-to-READ-to-PRECHARGE	I_{DD1}	1926	mA	1, 2
Precharge power-down current	I_{DD2P}	432	mA	1, 3
Precharge standby current	I_{DD2N}	1332	mA	1, 3
Precharge quiet standby current	I_{DD2Q}	1296	mA	1, 3
Active power-down current (Fast Exit)	I_{DD3P}	1152	mA	1, 3
Active standby current	I_{DD3N}	2088	mA	1, 3
Burst read operating current	I_{DD4R}	3006	mA	1, 2
Burst write operating current	I_{DD4W}	3042	mA	1, 2
Refresh current	I_{DD5B}	3276	mA	1, 2
Distributed Refresh current	I_{DD5D}	990	mA	1, 2
Self refresh temperature current: MAX T_c = 85°C	I_{DD6}	432	mA	1, 3
All banks interleaved read current	I_{DD7}	3996	mA	1, 2

Notes:
1 Value shown for DDR2 SDRAM only and are computed from values specified in the 2GBit component data sheet.
2 One module rank in the active IDD, the other rank in IDD2N.
3 All ranks in this IDD conditions.

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Table 14 - AC Timing Parameter and Operating Conditions

Parameter / Condition		Symbol	Min	Max	Units
Clock Timing					
Clock period average: DLL disable mode	T_C = 0°C to 85°C	^tCK (DLL_DIS)	2.5	7.8	ns
	T_C => 85°C to 95°C		2.5	3.9	
Clock periods average: DLL enable mode (CL = 4, CWL = 3)		^tCK (AVG)	3.0	<3.75	ns
Clock periods average: DLL enable mode (CL = 6, CWL = 4)		^tCK (AVG)	2.5	<3.0	ns
High pulse width average		^tCH (AVG)	0.48	0.52	^tCK
Low pulse width average		^tCL (AVG)	0.48	0.52	^tCK
Clock period jitter	DLL locked	^tJITper	-100	100	ps
	DLL locking	$^tJITper,lck$	-80	80	ps
Clock absolute period		^tCK (ABS)	^tCK (AVG) MIN + ^tJITper MIN	^tCK (AVG) MAX + ^tJITper MAX	ps
Clock absolute high pulse width		^tCH (ABS)	^tCH (AVG) MIN x ^tCK (AVG) MIN + $^tJIT(DUTY)$ MIN	^tCH (AVG) MAX x ^tCK (AVG) MAX + $^tJIT(DUTY)$ MAX	ps
Clock absolute low pulse width		^tCL (ABS)	^tCL (AVG) MIN x ^tCK (AVG) MIN + $^tJIT(DUTY)$ MIN	^tCL (AVG) MAX x ^tCK (AVG) MAX + $^tJIT(DUTY)$ MAX	ps
Clock half pulse width		^tHP	Lower of ^tCH(ABS) or ^tCL(ABS)	-	ps
Cycle-to-cycle jitter	DLL locked	^tJITcc	-200	200	ps
	DLL locking	$^tJITcc,lck$	-160	160	ps
Duty-cycle jitter		$^tJIT(DUTY)$	-100	100	ps
Cumulative error across	2 cycles	$^tERR2per$	-150	150	ps
	3 cycles	$^tERR3per$	-175	175	ps
	4 cycles	$^tERR4per$	-200	200	ps
	5 cycles	$^tERR5per$	-200	200	ps
	6-10 cycles	$^tERR(6-10per)$	-300	300	ps
	11-50 cycles	$^tERR(11-50per)$	-450	450	ps
DQ Input Timing					
Data setup time to DQS, /DQS	Base (specification)	^tDS	50	-	ps
					ps
Data hold time from DQS, /DQS	Base (specification)	^tDH	125	-	ps
					ps
Minimum data pulse width		^tDIPW	0.35	-	^tCK
DQ Output Timing					
DQS, /DQS to DQ skew, per access		^tDQSQ	-	200	ps
DQ output access time from CK, /CK		^tAC	-400	400	ps
DQ output hold time from DQS, /DQS		^tQH	^tHP - ^tQHS	-	ps
DQ Hold skew factor		^tQHS	-	300	ps
DQ High-Z time from CK, /CK		^tHZ	-	^tAC(MAX)	ps
DQ Low-Z time from CK, /CK		^tLZDQ	2 x ^tAC(MIN)	^tAC(MAX)	ps
DQ Strobe Input Timing					
DQS, /DQS rising to CK, /CK rising		^tDQSS	-0.25	0.25	^tCK
DQS, /DQS differential input low pulse width		^tDQSL	0.35	-	^tCK

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Parameter / Condition		Symbol	Min	Max	Units
DQS, /DQS falling setup to CK, /CK rising		tDSS	0.2	-	tCK
DQS, /DQS falling hold from CK, /CK rising		tDSH	0.2	-	tCK
DQS, /DQS differential input high pulse width		tDQSH	0.35	-	tCK
DQS, /DQS differential WRITE preamble		tWPRE	0.35	-	tCK
DQS, /DQS differential WRITE postamble		tWPST	0.4	0.6	tCK
Write command to DQS associated clock edges		WL	RL - 1		tCK
DQ Strobe Output Timing					
DQS, /DQS rising to/from CK, /CK		tDQSCK	-350	350	ps
DQS, /DQS Low-Z time		tLZDQS	tAC(MIN)	tAC(MAX)	ps
DQS, /DQS differential READ preamble		tRPRE	0.9	1.1	tCK
DQS, /DQS differential READ postamble		tRPST	0.4	0.6	tCK
Command and Address Timing					
CTRL, CMD, ADDR setup to CK, /CK	Base (specification)	tIS	175	-	ps
CTRL, CMD, ADDR hold from CK, /CK	Base (specification)	tIH	250	-	ps
Minimum CTRL, CMD, ADDR pulse width		tIPW	0.6	-	tCK
ACTIVATE to internal READ or WRITE delay		tRCD	12.5	-	ns
PRECHARGE command period		tRP	12.5	-	ns
ACTIVATE-to-PRECHARGE command period		tRAS	45	70k	ns
ACTIVATE-to-ACTIVATE command period		tRC	57.5	-	ns
ACTIVATE-to-ACTIVATE minimum period		tRRD	7.5	-	ns
Four ACTIVATE windows (1KB page size)		tFAW	35	-	ns
Write recovery time		tWR	15	-	ns
Internal WRITE-to-READ delay		tWTR	7.5	-	ns
READ-to-PRECHARGE time		tRTP	7.5	-	ns
/CAS-to-/CAS command delay		tCCD	2	-	tCK
Auto precharge write recovery + precharge time		tDAL	WR + tRP/tCK (AVG)	-	tCK
MODE REGISTER SET command cycle time		tMRD	2	-	tCK
MODE REGISTER SET command update delay		tMOD	0	12	tCK
OCD drive mode output delay		tOIT	0	12	ns

For part number IMM1G72D2RDD4AG-B25(I)

Parameter / Condition		Symbol	Min	Max	Units
Refresh Timing					
REFRESH-to-ACTIVATE or REFRESH command period		^{t}RFC	195	-	ns
Maximum refresh period	T_c<=85°C	-	64 (1X)		ms
	T_c>85°C		32 (2X)		
Maximum average periodic refresh	T_c<=85°C	^{t}REFI	-	7.8 (64ms/8192)	us
	T_c>85°C		-	3.9 (32ms/8192)	
Self Refresh Timing					
Exit self refresh to non-read command		^{t}XSNR	^{t}RFC+10	-	ns
Exit self refresh to read command		^{t}XSRD	200	-	ns
Minimum time clocks remain ON after CKE asynchronously drops LOW		^{t}DELAY	^{t}IS + ^{t}CKE (AVG) + ^{t}IH	-	ns
Power-Down Timing					
CKE MIN pulse width		^{t}CKE (MIN)	3	-	^{t}CK
Power-Down Exit Timing					
Exit precharge pown-down to any command		^{t}XP	2	-	^{t}CK
Exit active power down to read command		^{t}XARD	2	-	^{t}CK
Exit active power down to read command (slow exit, lower power)		^{t}XARDS	8 - AL	-	^{t}CK
ODT Timing					
R_{TT} turn-on from ODTL on reference		^{t}AON	^{t}AC(MIN)	^{t}AC(MAX) + 0.7	ns
R_{TT} turn-off from ODTL off reference		^{t}AOF	^{t}AC(MIN)	^{t}AC(MAX) + 0.6	ns
ODT turn-on delay		^{t}AOND	2	2	^{t}CK
ODT turn-off delay		^{t}AOFD	2.5	2.5	^{t}CK
Asynchronous R_{TT} turn-on delay (power-down with DLL off)		^{t}AONPD	^{t}AC(MIN) + 2	2 ^{t}CK + ^{t}AC(MAX) + 1	ns
Asynchronous R_{TT} turn-off delay (power-down with DLL off)		^{t}AOFPD	^{t}AC(MIN) + 2	2.5 ^{t}CK + ^{t}AC(MAX) + 1	ns
ODT to Power Down Mode Entry Latency		^{t}ANPD	3	-	^{t}CK
ODT to Power Down Mode Exit Latency		^{t}AXPD	8	-	^{t}CK

For part number IMM1G72D2RDD4AG-B25(I)

Table 15 - SPD Information

Byte NO.	Description	Note	Hex
0	Number of Serial PD Bytes written during module production	128	80
1	Total number of Bytes in Serial PD device	256 bytes	08
2	Fundamental Memory Type (FPM, EDO, SDRAM, DDR, DDR2…)	DDR2 SDRAM	08
3	Number of Row Addresses on this assembly	15	0F
4	Number of Column Addresses on this assembly	11	0B
5	Number of DIMM Ranks	30.0mm planar 2ranks	61
6	Data Width of this assembly	72bit	48
7	Reserved	Reserved	00
8	Voltage Interface Level of this assembly	SSTL _18	05
9	SDRAM Cycle time at Maximum Supported CAS Latency (CL), CL=X	2.5ns	25
10	SDRAM Access from Clock	0.4ns	40
11	DIMM configuration type (Non-parity, Parity or ECC)	ECC with Address / Command Parity	06
12	Refresh Rate/Type	7.8us	82
13	Primary SDRAM Width	x4	04
14	Error Checking SDRAM Width	x4	04
15	Reserved	Reserved	00
16	SDRAM Device Attributes: Burst Lengths Supported	4, 8	0C
17	SDRAM Device Attributes: Number of Banks on SDRAM Device	8 Banks	08
18	SDRAM Device Attributes: CAS Latency	4, 5, 6	70
19	DIMM Mechanical Characteristics	Undefined	00
20	DIMM Type Information	Registered DIMM	01
21	SDRAM Module Attributes	1 PLL, 2 Registors	05
22	SDRAM Device Attributes: General	Supports 50 Ohm ODTTs, weak driver	03
23	Minimum Clock Cycle at CLX-1	3.0ns	30
24	Maximum Data Access Time (tAC) from Clock at CLX-1	0.45ns	45
25	Minimum Clock Cycle at CLX-2	3.75ns	3D
26	Maximum Data Access Time (tAC) from Clock at CLX-2	0.5ns	50
27	Minimum Row Precharge Time (tRP)	9.5ns	3C
28	Minimum Row Active to Row Active delay (tRRD)	7.5ns	1E
29	Minimum RAS to CAS delay (tRCD)	12.75ns	3C
30	Minimum Active to Precharge Time (tRAS)	45ns	2D
31	Module Rank Density	4GB	04
32	Address and Command Input Setup Time Before Clock (tIS)	0.17ns	17
33	Address and Command Input Hold Time After Clock (tIH)	0.25ns	25
34	Data Input Setup Time Before Strobe (tDS)	0.05ns	05
35	Data Input Hold Time After Strobe (tDH)	0.12ns	12
36	Write Recovery Time	12.75ns	3C
37	Internal write to read command delay (tWTR)	7.5ns	1E
38	Internal read to precharge command delay (tRTP)	7.5ns	1E
39	Memory Analysis Probe Characteristics	Reserved	00
40	Extension of Byte 41 tRC and Byte 42 tRFC	-	00
41	SDRAM Device Minimum Active to Active/Refresh Time (tRC)	60ns	3C

Byte NO.	Description	Note	Hex
42	SDRAM Device Minimum Refresh to Active/Refresh Command Period (tRFC)	195ns	C3
43	SDRAM Device Maximum device cycle time (tCKmax)	8.0ns	80
44	SDRAM Device maximum skew between DQS and DQ signals (tDQSQ)	0.20ns	14
45	SDRAM Device Maximum Read Data Hold Skew Factor (tQHS)	0.30ns	1E
46	PLL Relock Time	15us	0F
47	Bits 7:4: Tcasemax, Bits 3:0: DT4R4W Delta	Tcasemax = 85°C Not support DT4R4W Delta	00
48	Thermal resistance of DRAM device package from top (case) to ambient (Psi T-A DRAM)	Not supported	00
49	DRAM Case Temperature Rise from Ambient due to Activate-Precharge/Mode Bits (DT0/Mode Bits)	Not defined	00
50	DRAM Case Temperature Rise from Ambient due to Precharge/Quiet Standby (DT2N/DT2Q)	Not supported	00
51	DRAM Case Temperature Rise from Ambient due to Precharge Power-Down(DT2P)	Not supported	00
52	DRAM Case Temperature Rise from Ambient due to Active Standby (DT3N)	Not supported	00
53	DRAM Case temperature Rise from Ambient due to Active Power-Down with Fast PDN Exit (DT3Pfast)	Not supported	00
54	DRAM Case temperature Rise from Ambient due to Active Power-Down with Slow PDN Exit (DT3Pslow)	Not supported	00
55	DRAM Case Temperature Rise from Ambient due to Page Open Burst Read/ DT4R4W Mode Bit (DT4R/DT4R4W Mode Bit)	Not supported	00
56	DRAM Case Temperature Rise from Ambient due to Burst Refresh (DT5B)	Not supported	00
57	DRAM Case Temperature Rise from Ambient due to Bank Interleave Reads with Auto-Precharge (DT7)	Not supported	00
58	Thermal Resistance of PLL Package from Top (Case) to Ambient (Psi T-A PLL)	Not supported	00
59	Thermal Resistance of Register Package from Top (Case) to Ambient (Psi T-A Register)	Not supported	00
60	PLL Case Temperature Rise from Ambient due to PLL Active (DT PLL Active)	Not supported	00
61	Register Case Temperature Rise from Ambient due to Register Active/Mode Bit (DT Register Active/Mode Bit)	Not supported	00
62	SPD Revision	1.3	13
63	Checksum for Bytes 0-62	-	41
64-71	Manufacturer's JEDEC ID Code	Reserved	Reserved
72	Module Manufacturing Location	Reserved	Reserved
73-90	Module Part Number	Reserved	Reserved
91-92	Module Revision Code	Reserved	Reserved
93-94	Module Manufacturing Date	Reserved	Reserved
95-98	Module Serial Number	Reserved	Reserved
99-127	Manufacturer's Specific Data	Reserved	Reserved
128-255	Open for customer use	Reserved	Reserved

Revision History

Revision	Descriptions	Release Date
1.0	Initial release	Sep, 2019

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