Product Specification | Rev. 1.0 | 2021

IMM1G72D2FBD4AG (Die Revision B)
8GByte (1G x 72 Bit)

8GB DDR2 Fully Buffered DIMM
RoHS Compliant Product

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Features

- 240-Pin Fully Buffered Dual-In-Line Memory Module
- Capacity: 8GB
- Maximum Data Transfer Rate: 6.40GB/Sec
- JEDEC-Standard
- Power Supply: V_{DD}, V_{DDQ} = 1.8±0.1V
- Bi-directional Differential Data-Strobe (Single-ended data-strobe is an optional feature)
- 72 Bit Data Bus Width with ECC
- Buffer interface with high-speed differential point-to-point link at 1.5 volt
- Channel error detection and reporting
- Channel fail over mode support
- Programmable CAS Latency (CL):
  - PC2-6400: 4, 5, 6
  - PC2-5300: 4, 5
- Programmable Additive Latency (Posted /CAS): 0, CL-2 or CL-1(Clock)
- Write Latency (WL) = Read Latency (RC) - 1
- Posted /CAS
- On-Die Termination (ODT)
- Off-Chip Driver (OCD) Impedance Adjustment
- ZQ Calibration Supported
- Burst Type (Sequential & Interleave)
- Burst Length: 4, 8
- Refresh Mode: Auto and Self
- 8192 Refresh Cycles / 64ms
- Serial Presence Detect (SPD) with EEPROM
- Gold Edge Contacts
- 100% RoHS-Compliant
- Standard Module Height: 30.35mm (1.20inch)

Table 1 - Ordering Information for RoHS Compliant Product

Part Number	Module Density	Configuration	# of Ranks	Module Type
IMM1G72D2FBD4AG-Bzzzy	8GB	1Gx72	2	8GB DDR2 Fully Buffered DIMM

Notes:
y: Operating Temperature
zzz: Speed Grade

Table 2 - Temperature Grade

Part Number	Temperature Grade	T_{case}
Blank	Commercial temperature	0°C to 95°C
I	Industrial temperature	-40°C to 95°C

Remark: Tcase is the case surface temperature on the center/top side of the DRAM. The refresh rate is required to double when 85 °C < Tcase <= 95 °C.

Table 3 - Speed Grade

Part Number	Speed Grade	Max. Clock Frequency (min. Clock Cycle time @ min. CAS Latency)
25	PC2-6400 (DDR2-800)	400MHz (2.5ns@CL=6)
3	PC2-5300 (DDR2-667)	333MHz (3.0ns@CL=5)

Table 4 - Memory Chip Information

Part Number	Base Device Brand	Base device	Voltage	Type	Chip Packing
IMM1G72D2FBD4AG-Bzzzy	I'M	IM2G04D2DBBG	1.8V	512Mx4	Lead Free

Part Number Decoder

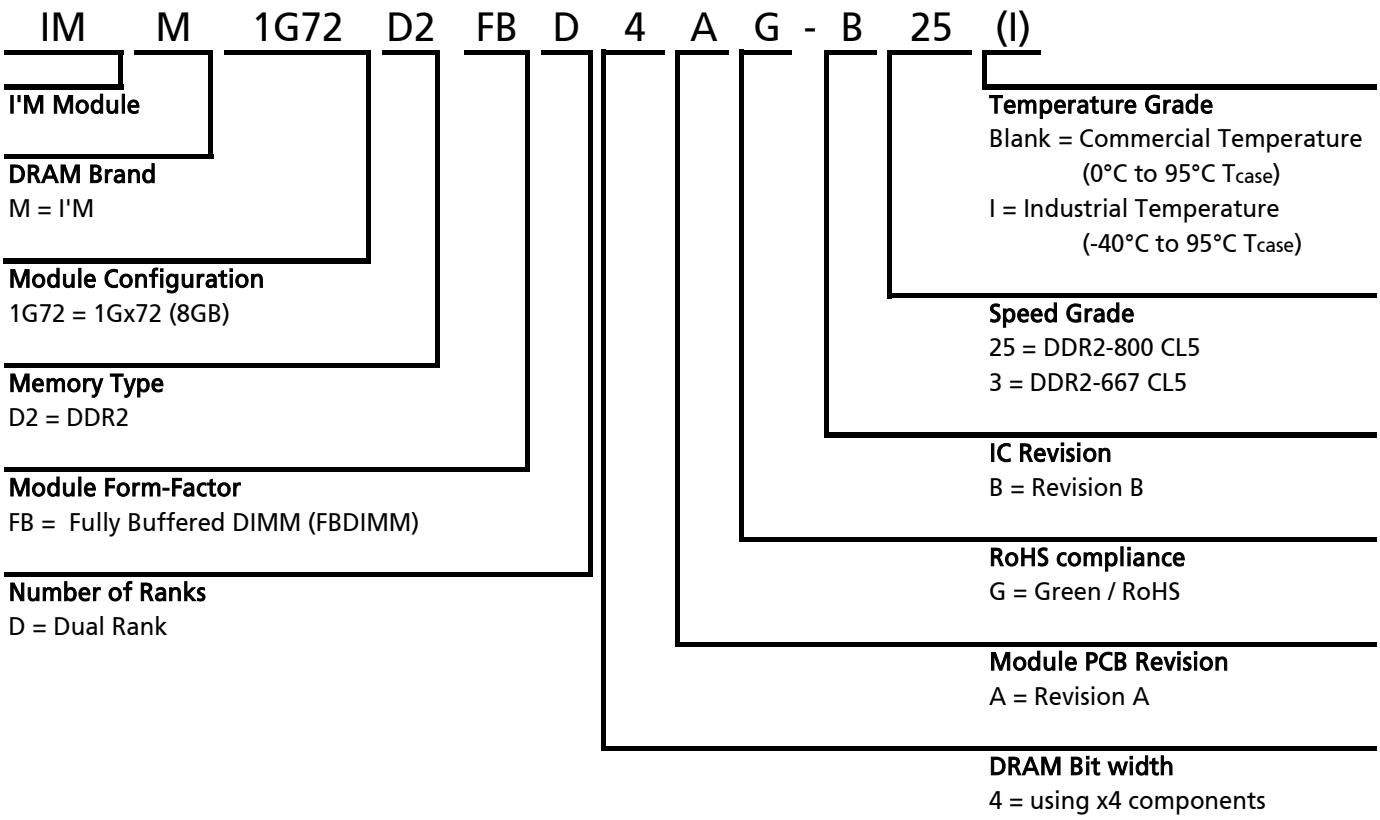

Table 5 - Addressing

Parameter	8GB
Refresh count	8K
Row address	32K A[14:0]
Device bank address	8 BA[2:0]
Device configuration	2Gb (512Mx4)
Column address	2K A[9:0], A11
Module rank address	2 /S[1:0]
Number of devices	36

Table 6 - Pin Assignment

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{DD}	121	V_{DD}	61	/PN9	181	/SN9
2	V_{DD}	122	V_{DD}	62	V_{SS}	182	V_{SS}
3	V_{DD}	123	V_{DD}	63	PN10	183	SN10
4	V_{SS}	124	V_{SS}	64	/PN10	184	/SN10
5	V_{DD}	125	V_{DD}	65	V_{SS}	185	V_{SS}
6	V_{DD}	126	V_{DD}	66	PN11	186	SN11
7	V_{DD}	127	V_{DD}	67	/PN11	187	/SN11
8	V_{SS}	128	V_{SS}	68	V_{SS}	188	V_{SS}
9	V_{CC}	129	V_{CC}	69	V_{SS}	189	V_{SS}
10	V_{CC}	130	V_{CC}	70	PS0	190	SS0
11	V_{SS}	131	V_{SS}	71	/PS0	191	/SS0
12	V_{CC}	132	V_{CC}	72	V_{SS}	192	V_{SS}
13	V_{CC}	133	V_{CC}	73	PS1	193	SS1
14	V_{SS}	134	V_{SS}	74	/PS1	194	/SS1
15	V_{TT}	135	V_{TT}	75	V_{SS}	195	V_{SS}
16	VID1	136	VID0	76	PS2	196	SS2
17	/RESET	137	DNU/M_Test	77	/PS2	197	/SS2
18	V_{SS}	138	V_{SS}	78	V_{SS}	198	V_{SS}
19	RFU	139	RFU	79	PS3	199	SS3
20	RFU	140	RFU	80	/PS3	200	/SS3
21	V_{SS}	141	V_{SS}	81	V_{SS}	201	V_{SS}
22	PN0	142	SN0	82	PS4	202	SS4
23	/PN0	143	/SN0	83	/PS4	203	/SS4
24	V_{SS}	144	V_{SS}	84	V_{SS}	204	V_{SS}
25	PN1	145	SN1	85	V_{SS}	205	V_{SS}
26	/PN1	146	/SN1	86	RFU	206	RFU
27	V_{SS}	147	V_{SS}	87	RFU	207	RFU
28	PN2	148	SN2	88	V_{SS}	208	V_{SS}
29	/PN2	149	/SN2	89	V_{SS}	209	V_{SS}
30	V_{SS}	150	V_{SS}	90	PS9	210	SS9
31	PN3	151	SN3	91	/PS9	211	/SS9
32	/PN3	152	/SN3	92	V_{SS}	212	V_{SS}
33	V_{SS}	153	V_{SS}	93	PS5	213	SS5
34	PN4	154	SN4	94	/PS5	214	/SS5
35	/PN4	155	/SN4	95	V_{SS}	215	V_{SS}
36	V_{SS}	156	V_{SS}	96	PS6	216	SS6
37	PN5	157	SN5	97	/PS6	217	/SS6
38	/PN5	158	/SN5	98	V_{SS}	218	V_{SS}
39	V_{SS}	159	V_{SS}	99	PS7	219	SS7
40	PN13	160	SN13	100	/PS7	220	/SS7
41	/PN13	161	/SN13	101	V_{SS}	221	V_{SS}
42	V_{SS}	162	V_{SS}	102	PS8	222	SS8
43	V_{SS}	163	V_{SS}	103	/PS8	223	/SS8
44	RFU	164	RFU	104	V_{SS}	224	V_{SS}
45	RFU	165	RFU	105	RFU	225	RFU
46	V_{SS}	166	V_{SS}	106	RFU	226	RFU
47	V_{SS}	167	V_{SS}	107	V_{SS}	227	V_{SS}
48	PN12	168	SN12	108	V_{DD}	228	SCK
49	/PN12	169	/SN12	109	V_{DD}	229	/SCK
50	V_{SS}	170	V_{SS}	110	V_{SS}	230	V_{SS}
51	PN6	171	SN6	111	V_{DD}	231	V_{DD}
52	/PN6	172	/SN6	112	V_{DD}	232	V_{DD}
53	V_{SS}	173	V_{SS}	113	V_{DD}	233	V_{DD}
54	PN7	174	SN7	114	V_{SS}	234	V_{SS}
55	/PN7	175	/SN7	115	V_{DD}	235	V_{DD}
56	V_{SS}	176	V_{SS}	116	V_{DD}	236	V_{DD}
57	PN8	177	SN8	117	V_{TT}	237	V_{TT}
58	/PN8	178	/SN8	118	SA2	238	V_{DDSPD}
59	V_{SS}	179	V_{SS}	119	SDA	239	SA0
60	PN9	180	SN9	120	SCL	240	SA1

Table 7 - Pin Description

Pin Name	Description	Pin Name	Description
SCK	System Clock Input, positive line[1]	/RESET	AMB reset signal
/SCK	System Clock Input, negative line[1]	V_{CC}	AMB Core Power and AMB Channel Interface Power
PN[13:0]	Primary Northbound Data, positive lines	V_{DD}	SDRAM Power and AMB DRAM I/O Power
/PN[13:0]	Primary Northbound Data, negative lines	V_{TT}	SDRAM Address/Command/Clock Termination Power (VDD/2)
PS[9:0]	Primary Southbound Data, positive lines	V_{SS}	Ground
/PS[9:0]	Primary Southbound Data, negative lines	V_{DDSPD}	EEPROM Power
SN[13:0]	Secondary Northbound Data, positive lines	SDA	EEPROM Data Input / Output
/SN[13:0]	Secondary Northbound Data, negative lines	SCL	EEPROM Clock Input
SS[9:0]	Secondary Northbound Data, positive lines	SA[2:0]	EEPROM Address Inputs, also used to select DIMM number in the AMB
/SS[9:0]	Secondary Northbound Data, negative lines	RFU	Reserved for Future use[2]
VID[1:0]	Voltage ID: These pins must be unconnected for DDR2-based Fully Buffered DIMMs. VID[0] is VDD value: OPEN=1.8V, GND=1.5V; VID[1] is VCC value: OPEN=1.5V, GND=1.2V.		
DNU, M_Test	The DNU / M_Test pin provides an external connection on R/Cs A-D for testing the margin of Vref which is produced by a voltage divider on the module .It is not intended to be used in normal system operation and must not be connected (DNU) in a system. This test pin may have other features on future card designs and if it does, will be included in this specification at that time.		

1. System Clock Signals SCK and /SCK switch at one half the DRAM CK, /CK frequency.
2. Eight pins reserved for forwarded clocks, eight pins reserved for future architecture flexibility.

Module Dimension

Figure 1 – 240 Pin DDR2 SDRAM Fully Buffered DIMM

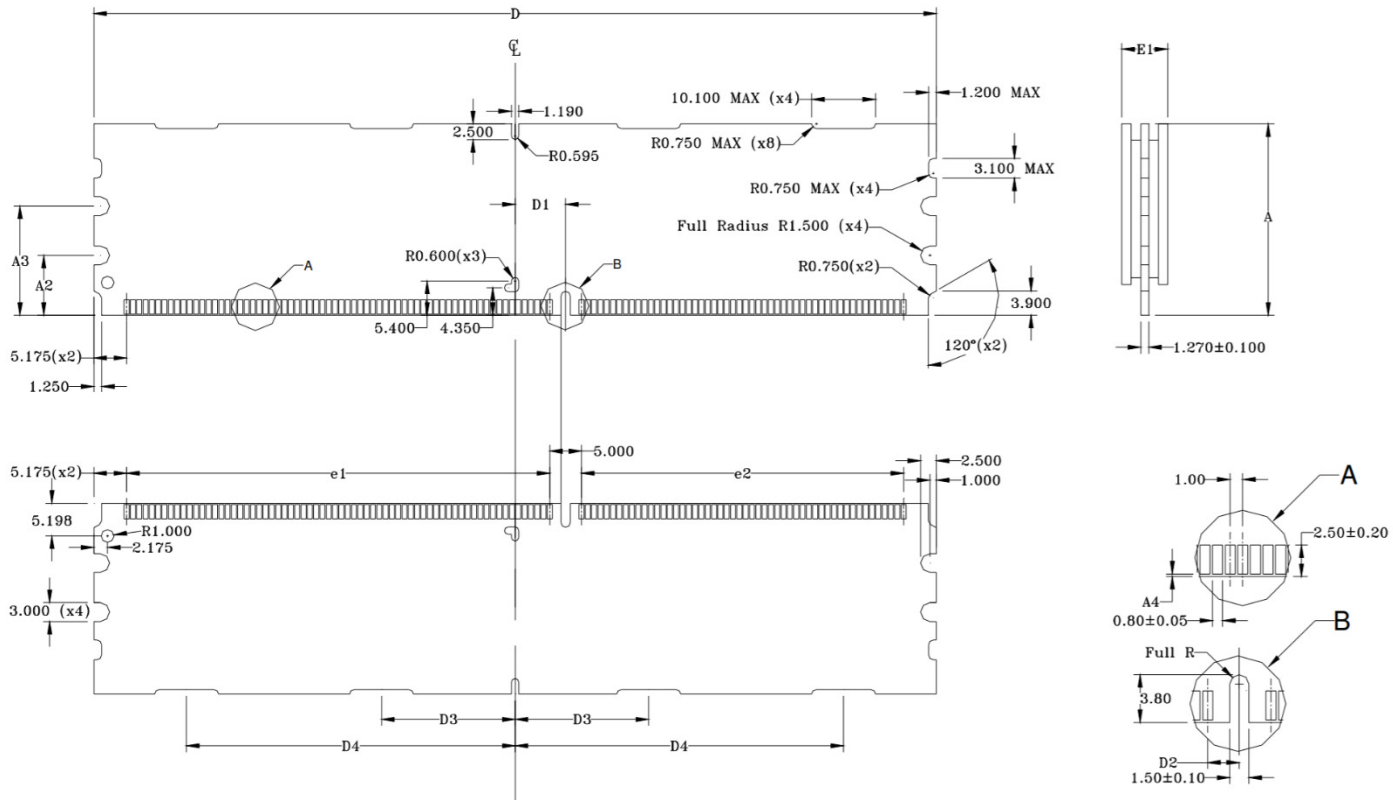

Table 8 - PCB Dimension			
Symbol	MIN	NOM	MAX
A	30.20	30.35	30.50
A2	9.50 Basic		
A3	17.30 Basic		
A4	0.05	0.20	0.35
D	133.20	133.35	133.50
D1	8.00 Basic		
D2	2.50 Basic		
D3	21.15 Basic		
D4	52.00 Basic		
e1	67.00 Basic		
e2	51.00 Basic		
E			8.00

Notes:

- All dimensioning and tolerancing conform to ASME Y14.5M-1994.
- Tolerances for all dimensions ±0.15 unless otherwise specified.
- All dimensions are in millimeters.

Revision History

Revision	Descriptions	Release Date
1.0	Initial release	Jun, 2021