ATP Velocity MV Industrial Temperature

SATA SSD Specification

Version 4.0

ATP Electronics, Inc.

CONTENT

Disclaimer ***1***

Revision History ***1***

1.0 ATP Velocity MV Industrial Temperature SATA SSD Overview ***2***

1.1 ATP Product Image *2*

1.2 Introduction *3*

1.3 Main Features *3*

1.4 Power Protector --- Data Integrity Under Power-cycling *4*

1.5 AutoRefresh Technology --Data Integrity Protection *4*

2.0 Product Specification ***5***

2.1 Block Diagram *5*

2.2 Environment Specifications *6*

2.3 IOPS[1] *6*

2.4 Maximum Read/Write Performance *7*

2.5 Electrical Characteristics *7*

2.6 Reliability *7*

2.7 Write/Erase Endurance[1] *8*

2.8 Certification and compliance *8*

3.0 SATA SSD Pin Assignment ***9***

3.1 Pin Location *9*

3.2 Pin Assignment *9*

4.0 Command Set ***10***

4.1 ATA Command Set *10*

4.2 Identity Device Data *12*

4.3 Smart Information *15*

4.3.1 Smart Subcommand Sets 15

4.3.2 SMART Read Data (Subcommand D0h) 16

4.3.3 SMART Attribute 17

4.4 SMART Command Transport *19*

4.4 Set Features *19*

5.0 Mechanical Information..... 19

5.1 Physical Dimension Specifications 19

5.2 Mechanical Form Factor (Units in mm) 20

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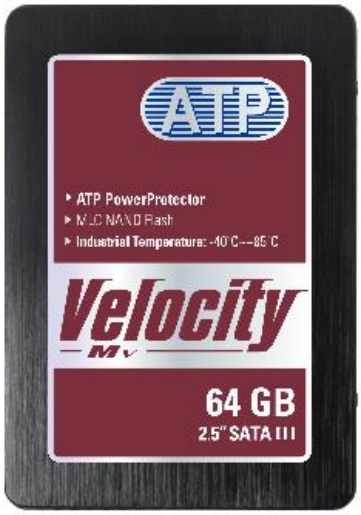
Revision History

Date	Version	Changes compared to previous issue
Mar. 7th, 2018	**4.0**	**- First Release**

1.0 ATP Velocity MV Industrial Temperature SATA SSD Overview

1.1 ATP Product Image



AF64GSMCJ-VADIP

Figure 1-1: ATP Product Image

Table 1-1: Capacities

ATP P/N	CAPACITY	Power Protector
AF64GSMCJ-VADIP	**64GB**	**Yes**

Note: GB = 1,000,000,000 Byte

1.2 Introduction

ATP Velocity MV Industrial Temperature 2.5” SSD is a best-in-class MLC SSD solution with enterprise-class features for cost-sensitive client environment. MV SSD offers outstanding performance and proven reliability, ideal for extreme performance, and consistent data integrity requirement, suited for POS, industrial computers, data center and industrial applications exposed to high shock and vibration environments.

1.3 Main Features

- Capacity 64GB
- MLC (Multiple Level Cell) NAND flash memory
- Operating temperature: -40℃ to 85℃
- Maximum performance: Sequential read up to 440 MB/s, sequential write up to 78 MB/s
- 2.5” form factor.
- Compliant with Serial ATA Revision 3.2
- 6Gb/s SATA V3.0 compliant and back compatible with SATA 1.5Gbps and SATA 3Gbps interface rate
- Hardware BCH ECC, correct up to 40-bit ECC per 1100 bytes of data
- Supports Native Command Queue (NCQ)
- SMART function support by ATA CMD
- Support TRIM command (Windows 7 and up, latest Linux Kernel)
- Support Firmware Live Update
- Temperature Sensor to Detect Device’s & Controller’s Temperatures
- Idle Clean FW Algorithm to Optimize Write Performance
- Enhanced endurance by Global wear-leveling & DRAM Flush Cache Efficiency
- Power Protector, data integrity under power-cycling
- NSA Compliant Secure Erase
- CE , FCC certification

1.4 Power Protector --- Data Integrity Under Power-cycling

The unstable power conditions of outdoor applications such as transportation, telecommunications/networking and embedded systems run the risk of data loss and drive corruption during a sudden power failure.

A hardware design power protection is the ideal configuration for power backup, ensuring a sufficient amount of reserve power during any power abnormalities and minimizing the consequent host re-designs for adding new features. During a sudden power failure, the abnormality is discovered by a power loss detection circuit and activates the power protection mechanism. The device then draws power from power protection reservoir, where the reserve power is stored. The reserve power gives enough time for the flash device to conclude the last writing command without losing any data.

1.5 AutoRefresh Technology --Data Integrity Protection

Over time the error bits accumulate to the threshold in the flash memory cell and eventually become uncorrectable despite using the ECC engine. In the traditional handling method, the data is moved to a different location in the flash memory; despite the corrupted data is beyond repaired before the transition.

The situation is worse in frequent read applications, such as navigation systems or OS boot-up devices. The map or operation system is preloaded into the storage media and there may be one time write and following by read operation only. Read disturbance is the result of electrical interference from multiple read operations in surrounding pages. After NAND flash accumulates 100,000 read cycles, uncorrectable ECC errors may occur in the affected pages which results in data failure in the same block.

To prevent data corruption, ATP memory product monitors the error bit levels in each read operation; when it reaches the preset threshold value, AutoRefresh is activated by programming the data into another block before the data is corrupted. After the re-programming operation is completed, the controller reads the data and compares the data/parity to ensure data integrity.

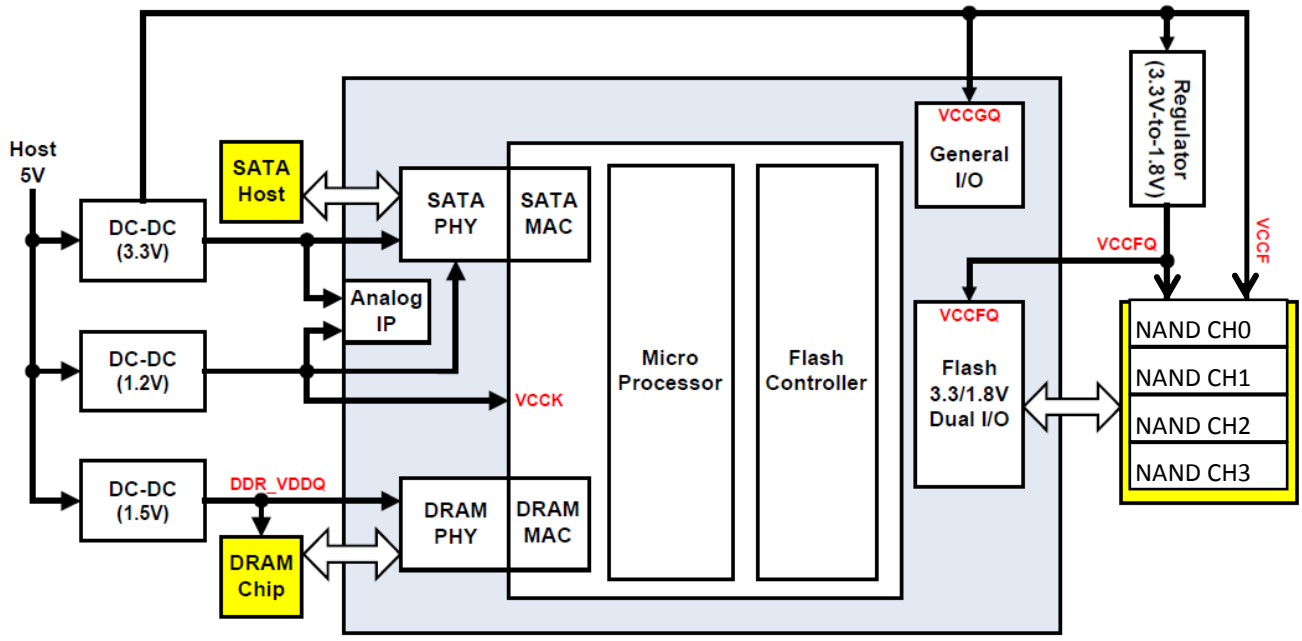
Owing to different user experiences, please contact ATP for AutoRefresh in real applications.

2.0 Product Specification

2.1 Block Diagram

ATP Velocity MV SATA SSD consists of below functional blocks. The advanced architecture is optimized to provide highest data reliability and transfer performance.

Figure 2-1:



2.2 Environment Specifications

Table 2-1

Type		Standard
Temperature	Operating	-40°C to 85°C
	Non-Operating	-40°C to 85°C
Humidity	Operating	25°C，8% to 95%, noncondensing
	Non-Operating	40°C，8% to 93%, noncondensing
Altitude	Operating	80,000 feet Max.
	Non-Operating	80,000 feet Max.

Note: The environment temperature specification is based on ATP internal reliability test condition under +85℃/-40℃ of sustaining burn-in temperature.

MIL-STD 810G Shock / Vibration:

Type		Standard
Vehicle Vibration Operating	Method 514.6, Figure 514.6C-3 Category4	Composite wheeled vehicle vibration exposure. Frequency: 5~500 Hz. Test duration: 1 hours x 3 axis
Aircraft Vibration	Figure 514.6D-3, Category 14	Helicopter vibration. Frequency: 10~500 Hz. Test duration: 1 hours x 3 axis.
Vibration Integrity	Figure 514.6E-1, Category 24	General minimum integrity exposure. Frequency: 20~2000 Hz. Test duration: 1 hours x 3 axis.
Mechanical Shock	Method 516.6, Figure 516.6-10	40G, 11 ms, saw-tooth pulse configuration, 6 faces with 3 shocks per axis.

2.3 IOPS[1]

Table 2-2

Type	Value
4K Random Read IOPS (QD32)	38,400
4K Random Write IOPS (QD32)	19,900

Note: Input/Output operations per second tested by Crystal Disk Mark on 64GB densities.

2.4 Maximum Read/Write Performance

Table 2-3

Type		64GB
Crystal Disk Mark	Sequential Read	440
	Sequential Write	78

System Configuration: Intel® *Core™ i7* processor, Gigabyte GA-Z97-D3H motherboard, Windows 7 Ultimate 64-bit

2.5 Electrical Characteristics

Table 2-4

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Supply voltage	V_{CC}	4.5	5.0	5.5	V	

Table2-5

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Sustained write power	P_W	1.0	1.2	1.8	W	RMS value
Sustained read power	P_R	1.0	1.1	1.5	W	RMS value
Idle power	P_S	0.38	0.6	0.6	W	RMS value

2.6 Reliability

Table2-6

Type	Value
MTBF (@ 25°C) [1]	>2,000,000 hours
Data Retention (@ 55°C)[2]	5 years (with 10% P/E cycle)
SATA connector's Durability[3]	500 cycles minimum. (Plug latch inoperative) Operation speed: maximum 200 cycles per hour.

Notes:

1. The Mean Time between Failures (MTBF) is calculated using a prediction methodology, Telcordia SR-332, which based on reliability data of the individual components in the MV. It assumes nominal voltage, with all other parameters within specified range.
2. Data retention value may vary across different temperature range and is experimental result to be used for reference.
3. The figures are based on EIA 364-09 standard to tested with backplane/blindmate application.

2.7 Write/Erase Endurance[1]

Table 2-7

Type	Value
SSD Endurance	64GB: 24.61 terabyte random write[2] 145.45 terabyte sequential write[3]

Notes:

1. Endurance for the MV can be predicted based on the usage conditions applied to the device, the internal NAND component cycles, the write amplification factor, and the wear leveling efficiency of the drive. TBW may vary depending on application, please contact ATP for TCO evaluation if specific usage type applies.
2. The calculation of random write endurance is based on JESD 219 enterprise workload.
3. The sequential write endurance calculation is based on pure sequential write at 128K transfer size in 4K alignment test pattern. TBW may vary depending on application, please contact ATP for TCO evaluation if specific usage type applies.

2.8 Certification and compliance

Table 2-8

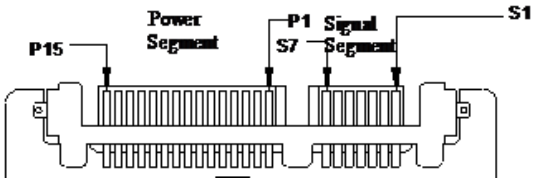
Mark/Approval	Documentation	Certification
CE	The CE marking (also known as CE mark) is a mandatory conformance mark on many products placed on the single market in the European Economic Area (EEA). The CE marking certifies that a product has met EU consumer safety, health or environmental requirements. CE stands for Conformité Européenne, "European conformity" in French.	Yes
FC	FCC Part 15 Class B was used for Evolution of United States (US) Emission Standards for Commercial Electronic Products, The United States (US) covers all types of unintentional radiators under Subparts A and B (Sections 15.1 through 15.199) of FCC 47 CFR Part 15, usually called just FCC Part 15	Yes

3.0 SATA SSD Pin Assignment

3.1 Pin Location

The following figure shows the pin location of the Velocity MV SATA SSD, the connector is with both signal and power segments.

Figure 3-1



3.2 Pin Assignment

There are total of 7 pins in the signal segment and 15 pins in the power segment. The pin definitions are shown in Table 3-1

Table 3-1

Group	Pin No.[1]	Function	Description
Signal Segment	S1	GND	Ground
	S2	A+	Differential signal pair A
	S3	A-	
	S4	GND	Ground
	S5	B-	Differential signal pair B
	S6	B+	
	S7	GND	Ground
Key & Spacing			
Power Segment	P1	NC/V_{33}	3.3V power (Not used)
	P2	NC/V_{33}	3.3V power (Not used)
	P3	DEVSLP	Enter/Exit DevSleep
	P4	GND	Ground
	P5	GND	Ground
	P6	GND	Ground
	P7	V5	5V power, pre-charge
	P8	V5	5V power
	P9	V5	5V power
	P10	GND	Ground
	P11	DAS/DSS#	Device Activity Signal / Disable

Power Segment			Staggered Spin-up
	P12	GND	Ground
	P13	NC/V12	12V power (Not used)
	P14	NC/V12	12V power (Not used)
	P15	NC/V12	12V power (Not used)

Note: All pins are in a single row, with a 1.27 mm (0.050") pitch.

4.0 Command Set

4.1 ATA Command Set

ATP Velocity MV supports the commands show in the following table

Table 4-1

Command	Code	Protocol
General Feature Set		
Execute Drive Diagnostic	90h	Device diagnostic
Flush Cache	E7h	Non-data
Flush Cache Ext	EAh	Non-data
Identify Device	ECh	PIO data-in
Initialize Drive Parameters	91h	Non-data
Read DMA	C8h	DMA
Read DMA Ext	25h	DMA
Read Log Ext	2Fh	PIO data-in
Read Multiple	C4h	PIO data-in
Read Sector(s)	20h or 21h	PIO data-in
Read Sector(s) Ext	24h	PIO data-in
Read Verify Sector(s)	40h or 41h	Non-data
Read Verify Sector(s) Ext	42h	Non-data
Set Feature	EFh	Non-data
Set Multiple Mode	C6h	Non-data
Write DMA	CAh	DMA
Write DMA Ext	35h	DMA
Write DMA Fua Ext	3Dh	DMA
Write Log Ext	3Fh	PIO data-out
Write Multiple	C5h	PIO data-out
Write Sector(s)	30h or 31h	PIO data-out
Write Sector(s) Ext	34h	PIO data-out
READ FPDMA QUEUED	60h	DMA
WRITE FPDMA QUEUED	61h	DMA
NOP	00h	Non-data

Command	Code	Protocol
Read Buffer	E4h	PIO data-in
Write Buffer	E8h	PIO data-out
Data Set Management	06h	DMA PIO data-out
Download Microcode	92h	
Power Management Feature Set		
Check Power Mode	E5h or 98h	Non-data
Idle	E3h or 97h	Non-data
Idle Immediate	E1h or 95h	Non-data
Sleep	E6h or 99h	Non-data
Standby	E2h or 96h	Non-data
Standby Immediate	E0h or 94h	Non-data
Security Mode Feature Set		
Security Set Password	F1h	PIO data-out
Security Unlock	F2h	PIO data-out
Security Erase Prepare	F3h	Non-data
Security Erase Unit	F4h	PIO data-out
Security Freeze Lock	F5h	Non-data
Security Disable Password	F6h	PIO data-out
SMART Feature Set		
SMART Disable Operation	B0h	Non-data
SMART Enable/Disable Autosave	B0h	Non-data
SMART Enable Operations	B0h	Non-data
SMART Return Status	B0h	Non-data
SMART Execute Off-Line Immediate	B0h	Non-data
SMART Read Data	B0h	PIO data-in
SMART Read Threshold	B0h	PIO data-in
SMART Read Log	B0h	PIO data-in
SMART Write Log	B0h	PIO data-out
SMART Save Attribute Values	B0h	Non-data
Host Protected Area Feature Set		
Read Native Max Address	F8h	Non-data
Read Native Max Address Ext	27h	Non-data
Set Max Address	F9h	Non-data
Set Max Address Ext	37h	Non-data
Set Max Set Password	F9h	PIO data-out

Command	Code	Protocol
Set Max Lock	F9h	Non-data
Set Max Freeze Lock	F9h	Non-data
Set Max Unlock	F9h	PIO data-out

4.2 Identity Device Data

Word Address	Default Value	Data Field Type Information
0	0040h	General Configuration
1	XXXXh	Default number of cylinders
2	0000h	Reserved
3	00XXh	Default number of heads
4	0000h	Obsolete
5	0240h	Obsolete
6	XXXXh	Default number of sectors per track
7-8	XXXXh	Number of sectors per card (Word 7 = MSW, Word 8 = LSW)
9	0000h	Obsolete
10-19	XXXXh	Serial number in ASCII (Left justified) with 12 or less characters
20	0002h	Obsolete
21	0002h	Obsolete
22	0000h	Obsolete
23-26	XXXXh	Firmware revision in ASCII (Left justified). Big Endian Byte Order in Word
27-41	XXXXh	Model number in ASCII (Left justified). Big Endian Byte Order in Word
42~46		Part number in ASCII (Right justified) preceded by the ANSI space character
47	8001h	Maximum number of sectors on Read/Write Multiple command
48	0000h	Trusted Computing feature set options
49	0F00h	Capabilities
50	4000h	Capabilities
51	0200h	PIO data transfer cycle timing mode
52	0000h	Obsolete
53	0007h	Field validity
54	XXXXh	Current numbers of cylinders
55	XXXXh	Current numbers of heads

Word Address	Default Value	Data Field Type Information
56	XXXXh	Current sectors per track
57-58	XXXXh	Current capacity in sectors (LBAs) (Word57=LSW, Word58=MSW)
59	0101h	Multiple sector setting
60-61	XXXXh	Total number of user addressable logical sectors for 28-bit commands (DWord)
62	0000h	Reserved
63	0207h	Multiword DMA transfer Supports MDMA Mode 0, 1, and 2
64	0003h	Advanced PIO modes supported
65	0078h	Minimum Multiword DMA transfer cycle time per word
66	0078h	Recommended Multiword DMA transfer cycle time
67	0078h	Minimum PIO transfer cycle time without flow control
68	0078h	Minimum PIO transfer cycle time with lORDY flow control
69	4000h	Additional supported
70~74	0000h	Reserved
75	0031	Queue depth
76	030E	Serial ATA capabilities Support Serial ATA Gen1 Support Serial ATA Gen2 Support Serial ATA Gen3 Supports Phy event counters log Support receipt of host-initiated interface power management requests Supports Native Command Queuing
77	0080h	Serial ATA additional capability DevSleep_to_ReducedPwerState
78	044C	Serial ATA features supported Supports Device Sleep Supports software settings preservation Device supports initiating power management
79	0040h	Serial ATA features enabled
80	03F0h	Major version number (ACS-2)
81	0000h	Minor version number
82	742Bh	Command sets supported 0
83	7500h	Command sets supported 1

Word Address	Default Value	Data Field Type Information
84	4023h	Command sets supported 2
85~87	XXXXh	Command set/feature enabled
88	007Fh	Ultra DMA supported and selected
89	0003h	Time required for Normal Erase mode Security Erase Unit command
90	0001h	Time required for Enhanced Erase mode Security Erase Unit command
91	0000h	Current advanced power management value
92	FFFEh	Master password identifier
93~99	0000h	Reserved
100~103	XXXXh	Maximum user LBA for 48-bit address feature set
104	0000h	Reserved
105	0100h	Maximum number of 512-byte blocks per Data Set Management command
106	5000	bit 12 = 1 to indicate that the Logical Sector Size field is valid
		Bit 14 = 1
		Bit 15 = 0
107~116	0000h	Reserved
117~118	0x800	Logical sector size
119~127	0000h	Reserved
128	0001h	Security status
129~159	XXXXh	Vendor specific
160	0000h	Power requirement description
161	0000h	Reserved
162	0000h	Key management schemes supported
163	0000h	CF Advanced True IDE Timing Mode Capability and Setting
164~168	0000h	Reserved
169	0001h	Data Set Management supported
170~205	XXXXh	Reserved
206	0x35	SCT Command Transport
207~216	XXXXh	Reserved
217	0001h	Non-rotating media(SSD)
218~221	0000h	Reserved
222	107Fh	Transport major revision (SATA Rev 3.1)
223~233	0000h	Reserved

Word Address	Default Value	Data Field Type Information
234	x0001	Minimum number of 512-byte data blocks per DOWNLOAD MICROCODE command for mode 03h
235	0x0200	Maximum number of 512-byte data blocks per DOWNLOAD MICROCODE command for mode 03h.
236~254	0000h	Reserved
255	XXXXh	Integrity word

4.3 Smart Information

ATP MV supports S.M.A.R.T. ATA feature set in IDE mode, AHCI mode.

4.3.1 Smart Subcommand Sets

In order to select a subcommand the host must write the subcommand code to the device's Features Register before issuing the SMART Function Set command. The subcommands are listed below.

Table 4-3

Command	Command Code
SMART READ DATA	D0h
SMART READ ATTRIBUTE THRESHOLD	D1h
SMART ENABLE/DISABLE AUTOSAVE	D2h
SMART SAVE ATTRIBUTE VALUES	D3h
SMART EXECUTE OFF-LINE IMMIDIATE	D4h
READ LOG	D5h
WRITE LOG	D6h
SMART ENABLE OPERATIONS	D8h
SMART DISABLE OPERATIONS	D9h
SMART RETURN STATUS	DAh

Note: If the reserved size is below a threshold, status can be read from the Cylinder Register using the Return Status command (DAh)

4.3.2 SMART Read Data (Subcommand D0h)

The following 512 bytes make up the device SMART data structure. Users can obtain the data using the “Read Data” command (D0h).

Table 4-4

Byte	F/V	Description
0~1	X	Revision code
2~361	X	Vendor Specific
362	V	Off-line data collection status
363	X	Self-test execution status byte
364~365	V	Total time in seconds to complete off-line data collection activity
366	X	Vendor Specific
367	F	Off-line data collection capability
368~369	F	SMART capability
370	F	Error logging capability: 7-1 = Reserved 0 -1 = Device error logging supported
371	X	Vendor Specific
372	F	Short self-test routine recommended polling time (in minutes)
373	F	Extended self-test routine recommended polling time (in minutes)
374	F	Conveyance self-test routine recommended polling time (in minutes)
375~385	R	Reserved
386~395	F	Firmware Version/Date Code
396~397	F	Reserved
398~399	F	Reserved
400~408	F	SMI2246EN
409~415	X	Vendor specific
416	F	Reserved
417	F	Program/write the strong page only
418~419	V	Number of spare block

420~423	V	Average erase count
424~510	X	Vendor Specific
511	V	Data structure checksum

Notes:

1. F=content (byte) is fixed and does not change
2. V=content (byte) is variable and maybe change depending on the state of the device or the command executed by the device
3. X= content (byte) is vendor specific and maybe fixed or variable
4. R=content (byte) is reserved and shall be zero

4.3.3 SMART Attribute

The following table defines the vendor specific data in byte 2 to 361 of the 512-byte SMART data.

ID	Value (hex)	Raw Attribute Value							Attribute Name
1	01	LSB	MSB	0	0	0	0	0	Raw Read Error Count (0x01)
5	05	LSB	MSB	0	0	0	0	0	Reallocated Flash Blocks Count
9	09	LSB			MSB	0	0	0	Power On Hours (0x09)
12	0C	LSB			MSB	0	0	0	Normal Power On/Off count
14	0E	LSB			MSB	0	0	0	Device Physical Capacity (0x0E)
15	0F	LSB			MSB	0	0		Device User Capacity (0x0F)
16	10	LSB	MSB	0	0	0	0	0	Initial Spare blocks (0x10)
17	11	LSB	MSB	0	0	0	0	0	Remaining Spare Blocks at Current Time (0x11)
100	64	LSB			MSB	0	0	0	Total Erase Count
160	A0	LSB			MSB	0	0	0	Uncorrectable Sector Count When Read/Write
172	AC	LSB	MSB	0	0	0	0	0	Total Block Erase Failure (0xAC)

ID	Value (hex)	Raw Attribute Value							Attribute Name
173	AD	LSB			MSB	0	0	0	Maximum Erase Count (0xAD)
174	AE	LSB			MSB	0	0	0	Unexpected Power Loss Count
175	AF	LSB			MSB	0	0	0	Average Erase Count
181	B5	LSB			MSB	0	0	0	Total Block Program Failure
187	BB	LSB			MSB	0	0	0	Reported Uncorrectable Errors (0xBB)
194	C2	LSB MSB	0	0	0	0	0	0	Device Temperature (0xC2)
195	C3	LSB			MSB	0	0	0	Hardware ECC Recovered
197	C5	LSB MSB	0	0	0	0	0	0	Current Pending Block Count (0xC5)
198	C6	LSB			MSB	0	0	0	Offline Surface Scan (0xC6)
199	C7	LSB	MSB	0	0	0	0	0	SATA FIS CRC Errors
202	CA	LSB			MSB	0	0	0	Percentage of Drive Life Used
205	CD	LSB			MSB	0	0	0	Thermal Asperity Rate (TAR)
231	E7	LSB MSB	0	0	0	0	0	0	Controller Temperature
234	EA	LSB						MSB	Total Sectors Read from NAND Flash
235	EB	LSB						MSB	Total Sectors Bytes Written to Device
241	F1	LSB						MSB	Total NAND Sectors Written to NAND Flash
242	F2	LSB						MSB	Total Sectors Read from Device

ID	Value (hex)	Raw Attribute Value						Attribute Name
248	F8	LSB MSB	0	0	0	0	0	0	Remaining Life %
249	F9	LSB MSB	0	0	0	0	0	0	Spare Block Remaining

4.4 SMART Command Transport

Action Code (hex)	Description
0003h	Error recovery control (the time needed to recover)
0004h	Features control
0005h	SCT data tables

4.4 Set Features

Feature code (hex)	Description
2	Enable write cache
66	Disable reverting to Power-On defaults
82	Disable write cache
CC	Enable reverting to Power-On defaults

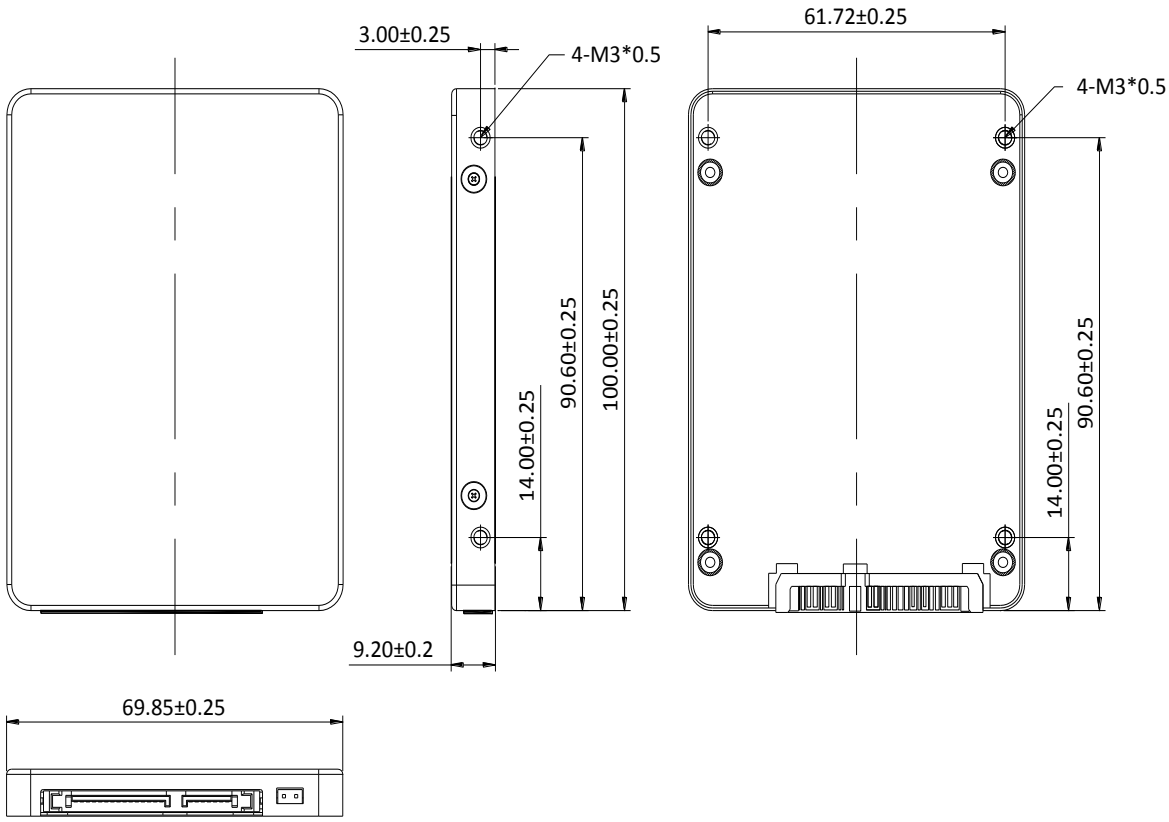
5.0 Mechanical Information

5.1 Physical Dimension Specifications

Table 5-1

Type		Value
MV SATA SSD	Length	100.00 mm +/- 0.25mm
	Width	69.85 mm +/- 0.25 mm
	Thickness	9.20 mm +/- 0.20mm

5.2 Mechanical Form Factor (Units in mm)



ATP TAIWAN(HQ)
TEL: +886-2-2659-6368
FAX: +886-2-2659-4982
sales-apac@atpinc.com

ATP USA
TEL: +1-408-732-5000
FAX: +1-408-732-5055
sales@atpinc.com

ATP JAPAN
TEL: +81-03-6206-8097
FAX: +81-03-6206-8098
sales-japan@atpinc.com

ATP EUROPE
TEL: +49-89-374-9999-0
FAX: +49-89-374-9999-29
sales-europe@atpinc.com

ATP CHINA
TEL: +86-21-5080-2220
FAX: +86-21-5080-2219
sales@cn.atpinc.com

www.atpinc.com